New Insights on Output Capacitance Losses in Wide-Band-Gap Transistors

Mohammad Samizadeh Nikoo, Member, IEEE, Armin Jafari, Nirmana Perera, Student Member, IEEE, and Elison Matioli, Member, IEEE

Abstract—The low ON-resistance of wide-band-gap (WBG) transistors is a key feature for efficient power converters, however, the anomalous loss in their output capacitance (C_{OSS}) severely limits their performance at high switching frequencies. Characterizing C_{OSS}-losses based on large-signal measurement methods requires an extensive effort, as separate measurements are needed at different operation points, including voltage-swing, frequency, and dv/dt. Furthermore, there is a practical trade-off in the maximum voltage and frequency applied to the device. Here we introduce a new circuit model, including an effective C_{OSS} and a frequency-dependent series-resistance, along with a simple small-signal method to fully characterize C_{OSS}-losses in WBG transistors. The method accurately predicts C_{OSS}-losses at any voltage-swing or frequency. Contrary to other methods, this technique directly leads to a general identification of C_{OSS}-losses at different operation points, revealing new insights on dependence of C_{OSS}-losses in WBG transistors, especially the dependence of E_{Diss} on voltage and frequency. Based on the proposed approach, the issue of C_{OSS}-losses in enhancement-mode GaN and SiC transistors was assigned to the limited quality-factor of C_{OSS}. The precise characterization of C_{OSS}-losses proposed in this letter is essential for designing efficient high-frequency power converters.

Index Terms—Output capacitance, C_{OSS}, Energy loss, E_{Diss}, Nonlinear resonance, Superjunction, SiC, GaN, Cascode.

I. INTRODUCTION

The non-recoverable energy loss associated with resonantly charging and discharging the output capacitance (C_{OSS}) of some of the advanced transistors and diodes considerably limit their performance in power converters, especially those operating at high frequencies [1]-[11]. An unexpected power loss in soft-switched power converters based on Si superjunction (SJ) MOSFETs, especially those with low specific R_{ON}, initiated studies on their large-signal C_{OSS}, where a non-symmetric charging and discharging processes was observed. Measurements with Sawyer-Tower (ST) method showed a frequency-independent C_{OSS}-loss due to the charge-trapping in SJ devices [8]-[11].

The lower-than-expected efficiencies in soft-switching power converters based on wide-band-gap (WBG) transistors, again initiated investigations on C_{OSS}-losses [12]. Zulauf et al. characterized C_{OSS} charging/discharging energy dissipation (E_{Diss}) in GaN transistors using Sawyer Tower (ST) method, where the results showed frequency-dependent losses [2]. Guacci et al. used a thermal approach to study C_{OSS}-losses in GaN transistors and observed dv/dt-dependent energy dissipation [3]. The ST-based E_{Diss} measurement of some of the commercial SiC transistors, however, presented a weak dependence on frequency and dv/dt [1].

Although several measurements showed an effect from voltage-swing, frequency and dv/dt on C_{OSS} -losses in SiC and enhancement-mode GaN transistors, the dependence of E_{Diss} on these parameters is still not clear [3]. Zulauf et al. [1] used the empirical relation

$$E_{Diss}^{Ref[1]} = k \cdot f^\alpha \cdot V^\beta$$

(1)

to fit the experimental data, where f is the frequency, V is the charging voltage, and k, \alpha, and \beta are constants. For some of the evaluated transistors, values of \alpha < 1 and \beta < 2 were obtained [13]. Although curve fitting from large-signal measurements shows the behavior of C_{OSS}-losses, it requires excessive experiments with high-voltage and high-frequency power amplifiers at several operation points at different voltages and frequencies. Moreover, the need for a high-voltage RF power amplifier (PA) can severely limit the maximum voltage and frequency applied to the device under test (DUT).

In this work we propose a small-signal modeling approach to extract large-signal C_{OSS}-losses of WBG transistors on a wide range of operation points. The device is simply modeled by a nonlinear capacitance C_{OSS} in series with a frequency-dependent resistance R_s. This modeling decouples the frequency and voltage dependence of losses, enabling to solve a large-signal problem with a small-signal approach. Using an impedance measurement to measure values of R_s at different frequencies, together with the presented output capacitance versus voltage from datasheets, we present a general relationship for C_{OSS}-losses in different voltages and frequencies. As a result, just one simple small-signal measurement (instead of several different measurements in large-signal methods) leads to a general view of the C_{OSS}-losses. The method does not suffer from some of the shortcomings of large-signal measurements such as limitation in applied voltage/frequency (e.g. due to power amplifier), or signal distortion at high-frequencies. The proposed method gives insights on dependence of E_{Diss} on frequency, voltage, and dv/dt value.

II. MODEL

Fig. 1(a) shows a model for output capacitance of transistors, including a nonlinear capacitance C_{OSS} in series with resistance...
$R_S$ and in parallel with resistance $R_P$, representative for losses at high and low frequencies, respectively. The quality-factor ($Q$-factor) of output capacitance can be defined as [see Figs. 1(b) and (c)]

$$Q = \frac{1}{R_S C_{OSS} \omega + (R_P C_{OSS} \omega)^{-1}}$$

(2)

The effect of $R_P$ (mainly corresponding to the leakage current) is dominant at DC, while $R_S$ significantly contributes to the switching dynamics and $C_{OSS}$-losses. As illustrated in Fig. 1(d), small-signal measurements show a considerable lossy behavior for $C_{OSS}$ of WBG transistors. For instance, the levels of losses are considerably higher than a reference low-loss mica capacitor. The small-signal extracted values of losses for frequencies higher than 1 MHz, are in range of 1-10% which is in agreement with the previously measured large-signal losses [1], [2]. This indicates the possibility of evaluating large-signal losses with a proper small-signal modeling. Fig. 1(d) also shows that for frequencies higher than 1 MHz (which covers the switching bandwidth of WBG transistors), the $Q$-factor of all the considered transistors is limited by $R_S$.

For a linear capacitor with frequency-independent $R_S$ and $R_P$, (2) fully describes the charging/discharging energy dissipation as

$$E_{DISS} = \frac{\pi}{2Q} E_{OSS}$$

(3)

where $E_{OSS}$ is the total energy stored in $C_{OSS}$. In practice, however, $C_{OSS}$ is nonlinear and $R_S$ and $R_P$ can change with frequency [see Figs. 1(b) and 1(c)]. The non-unity slope of the $Q$-factor versus frequency for several different WBG transistors (Table I), shown in Fig. 1(d) (measured with Keysight E4990A impedance analyzer, with a very high accuracy), confirms the frequency-dependent nature of $R_S$ and $R_P$.

We use the model presented in Fig. 1(a) to extract $C_{OSS}$ charging/discharging energy dissipation. As mentioned, $R_S$ is the origin of $C_{OSS}$-losses in switching dynamics, as $R_P$ just limits the $Q$-factor at low frequencies. By applying voltage $v(t)$ to the output capacitance, and considering $R_S$ as a perturbation element, the power loss in $R_S$ can be written as

$$P_{loss} = R_S (C_{OSS} \frac{dv}{dt})^2$$

(4)

Assuming $v(t)$ represents a switching transient from 0 to $V$, the total energy loss during a single switching transient time $t_{SW}$ is

$$E_{loss} = \int_0^{t_{SW}} R_S (C_{OSS} \frac{dv}{dt})^2 dt$$

(5)

In a charging and discharging process, however, $E_{loss}$ is dissipated two times ($E_{DISS} = 2E_{loss}$). Considering a constant switching-speed $dv/dt \equiv V/t_{SW}$, which is very accurate for trapezoidal waveforms and also can be used for sinusoidal waveforms, we write

$$E_{DISS} = 2R_S (\frac{dV}{dt}) \int_0^V C_{OSS} dv$$

(6)

which clearly shows $dv/dt$-dependence of $C_{OSS}$-losses [2]-[4]. Equation (6) can be rewritten as

$$E_{DISS} = 2R_S (\frac{dV}{dt}) V C_{OSS}^{eff}$$

(7)

in which we introduced the new term $C_{OSS}^{eff}$ which is the root mean square (rms) of $C_{OSS}$ from 0 to $V$, representing the average $C_{OSS}$ value that contributes to power dissipation in the device output capacitance

$$C_{OSS}^{eff} = \frac{1}{V} \int_0^V C_{OSS}^2 dv$$

(8)

One can use $f = 1/(2t_{SW})$ to rewrite (6) as

$$E_{DISS} = 4R_S f V^2 C_{OSS}^{eff}$$

(9)

Comparing (9) with the experimental model (1) reveals two main points:

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**Table I**

<table>
<thead>
<tr>
<th>No.</th>
<th>Voltage and current rating</th>
<th>$C_{OSS}^{**}$</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td>Voltage (V)</td>
<td>Current (A)</td>
</tr>
<tr>
<td>M1</td>
<td>1200</td>
<td>36</td>
</tr>
<tr>
<td>M2</td>
<td>650</td>
<td>30</td>
</tr>
<tr>
<td>M3</td>
<td>650</td>
<td>93</td>
</tr>
<tr>
<td>M4</td>
<td>600</td>
<td>31</td>
</tr>
<tr>
<td>M5</td>
<td>100</td>
<td>90</td>
</tr>
<tr>
<td>M6</td>
<td>1700</td>
<td>4</td>
</tr>
<tr>
<td>M7</td>
<td>600</td>
<td>13</td>
</tr>
<tr>
<td>M8</td>
<td>1200</td>
<td>55</td>
</tr>
</tbody>
</table>

* Continuous current at 25 °C.
** Reported capacitance at 2/3 of voltage rating, measured at 1 MHz.
1) \( \alpha = 1 \) for a fixed and frequency-independent \( R_s \), however, non-unity values of \( \alpha \) have been reported in [2] and [13]. This agrees with the measurement results presented in Fig. 1(d), showing frequency-dependent \( R_s \).

2) The obtained values of \( \beta \), extracted by curve fitting in [13], were always less than 2. This is in agreement with (9) since when rising the voltage \( V \), the rms value of \( C_{OSS} \) decreases. As a result, although square of \( V \) is seen in (9), the \( C_{OSS} \)-related term leads to a \( \beta < 2 \).

### III. \( C_{OSS} \)-LOSS EVALUATION

Here we show how large-signal \( C_{OSS} \)-losses can be extracted from the small-signal model. This section also validates the applicability of the proposed method to evaluate \( C_{OSS} \)-losses, by comparing the extracted \( E_{DISS} \) values with the ST method [1], [2]. The first step to extract the general relation of (9) is to obtain the effective \( C_{OSS} \). This can be done by using data reported in datasheets. Figs. 2(a) and (b) show the reported \( C_{OSS} \) in datasheet of transistors M1 (36-A-rated SiC FET with \( R_{ON} = 80 \, \text{m} \Omega \)) and M2 (30-A-rated e-mode GaN HEMT with \( R_{ON} = 50 \, \text{m} \Omega \)), respectively. The effective \( C_{OSS} \) values were obtained using (8) [see Figs. 2(a) and (b)]. One can directly use these values, however, here we applied a curve fitting to obtain closed-form relations [dashed lines in Figs. 2(a) and (b)]:

\[
C_{eff}^{\text{OSS}} = (2850 \, \text{pF}) \cdot (V \, [\text{V}])^{-0.38} \tag{10}
\]

and

\[
C_{eff}^{\text{OSS}} = (2350 \, \text{nF}) \cdot (V \, [\text{V}])^{-0.42} \tag{11}
\]

for M1 and M2, respectively.

After extraction of the effective \( C_{OSS} \), the series resistance \( R_s \) was measured using a Keysight E4990A impedance analyzer [see Fig. 2(c)]. The \( R_s \), as a key element in \( C_{OSS} \)-losses, as a function of frequency is not typically reported by manufacturers.

\[
R_s = 11 f^{-0.91} \quad \text{for M1 (SiC)} \quad \text{and} \quad R_s = 2.2 f^{-0.8} \quad \text{for M2 (GaN)}.
\]

in datasheets. Fig. 2(d) illustrates the \( R_s \) for transistors M1 and M2 (solid lines). Unlike \( C_{OSS} \), which is strong function of voltage, \( R_s \) is almost constant with voltage; and therefore it can be assumed as linear parameter. On the other hand, \( C_{OSS} \) is not a function of frequency, while \( R_s \) is highly frequency-dependent [see Fig. 2(d)]. For M1 and M2 we have

\[
E_{DISS} = 0.357 \times f^{0.9} \times V^{1.24} \quad [\text{nJ}] \quad \text{for M1 (SiC)} \quad \text{and} \quad E_{DISS} = 0.049 \times f^{0.2} \times V^{1.16} \quad [\text{nJ}] \quad \text{for M2 (GaN)}
\]

where \( f \) and \( V \) are in MHz and Volts, respectively, showing losses at different operation points just by performing two measurements. The obtained relations were verified with measurement results using ST method with sinusoidal waveforms performed at 1 MHz for M1 [1] and at 10 MHz for M2 [2]. As shown in Fig. 3, good agreements were obtained for both transistors. It should be noted that the level of losses in these transistors are considerably different, showing the applicability of the proposed approach to extract \( C_{OSS} \)-losses for a wide range of \( E_{DISS} \) values.

### IV. DISCUSSION

Despite several experimental works on \( C_{OSS} \)-losses in WBG transistors, the dependence of \( E_{DISS} \) on frequency is not completely clear. Some transistors showed strong dependence of \( E_{DISS} \) on frequency, while for some other transistors it was very weak. The same observations can be seen for \( dv/dr \)-dependence. For some transistors, even lower \( E_{DISS} \) values were obtained for higher \( dv/dr \) values [1]. The proposed approach, however, clears the dependence of \( E_{DISS} \) on the frequency and \( dv/dr \).

Based on (9) \( E_{DISS} \sim R_s (f) \times f \), which shows the frequency-dependence of \( C_{OSS} \)-losses. Fig. 4 presents the \( E_{DISS} \)
GaAs (integrated with a low-voltage Si device) devices showed considerably higher loss for voltages larger than ~200 V [2], [4]. As a result, one can separately characterize frequency-independent (using ST method at the frequency corresponding to peak of $Q$-factor) and frequency-dependent (using the proposed method) $C_{OSS}$-losses. Adding these different component gives the general behavior of energy dissipation in the output capacitance.

Based on the proposed model, it is suggested to manufacturers to present $R_S$-versus-frequency (at least for frequencies above 1 MHz) for WBG transistors. This curve, together with $C_{OSS}^{\text{eff}}$ gives a general view on $C_{OSS}$-losses.

V. CONCLUSION

We proposed a new method to extract $C_{OSS}$-losses for WBG transistors at different voltages and time/frequency frames, just by performing one small-signal measurements: $R_S$-versus-frequency. This measurement together with the reported $C_{OSS}$-versus-$V_{DS}$ reveals the general $C_{OSS}$-loss behavior of the device. The method helps to clear the voltage and frequency dependence of $E_{\text{DISS}}$, and can be used to compare and benchmark different semiconductor devices. The results also led to a categorization of $C_{OSS}$-loss in different types of transistors. The $E_{\text{DISS}}$ in e-mode GaN and SiC transistors is mainly caused by the limited $Q$-factor of $C_{OSS}$, which was not observed in SJ and cascode devices. The generality and robustness of this method make it possible to quantify $C_{OSS}$-losses of WBG transistors as a crucial source of losses in soft-switch power converters, especially those operating at high frequencies.

REFERENCES


