1/f Noise in Fully Integrated Electrolytically Gated FinFETs with Fin Width Down to 20nm

Koen Martens, Bert Du Bois, Yong Kong Siew, Anshul Gupta, Anabela Veloso, Emmanuel Dupuy, Dunja Radisic, Efrain A. Sanchez, Willem Van Roy, Simone Severi, Eddy Simoen
Imec, Leuven, Belgium, koen.martens@imec.be

***Abstract*—The low frequency noise of nanoscale electrolytically gated FETs will determine the ISFET or BioFET sensor signal-to-noise ratio and is hence of key importance for FET-based biosensing applications. We report on the 1/f noise of fully integrated electrolytically gated FETs fabricated in a 300mm fabrication facility with fin widths down to 20nm. For a 20nm wide, 10µm long device we observe a gate referred noise Power Spectral Density (PSD) down to ~1x10^{-10}V^2/Hz at 10Hz, which is significantly lower than previously reported for electrolytically gated top-down fabricated FETs. We find the gate referred noise PSD to increase with increasing overdrive, indicating that lower overdrive is better for sensor signal-to-noise ratio.**

Keywords—ISFET, BioFET, FinFET, 1/f noise, pink noise

In this work the low frequency noise of electrolytically gated pMOS finFETs was characterized. The inversion mode pMOS finFET devices were fully fabricated in a 300mm processing facility in a process derived from a solid gate finFET process [1]. Fin widths down to 20nm were reached. Unlike MOSFETs, ISFETs (or bioFETs) use an electrolyte instead of metal or polysilicon as gate electrode. The devices had a 4nm SiON gate dielectric exposed to a 15mM phosphate buffered saline (PBS) electrolyte solution contacted by a Ag/AgCl electrode.

To accommodate the electrolyte a circular silicone flow cell with diameter 8 mm and depth 1 mm (by Grace Bio-Labs) was mounted on the die (DUT). The flow cell was connected to a flow-through true Ag/AgCl reference electrode (Microelectrodes Inc). The reference electrode contains a Ag/AgCl wire in contact with a 3 M KCl solution, separated from the buffer solution flowing in the flow-through part by a ceramic frit. The connections were made using polyvinyl chloride (PVC) and polytetrafluoroethylene (PTFE) tubes with inner and outer diameter of 1/16 inch x 1/8 inch (for PVC) and 0.023 inch x 1/16 inch (for PTFE), connected to a syringe containing the diluted PBS buffer solution. A Keysight E4727A low frequency noise analyzer was used which can measure noise down to 0.67 nV/ $\sqrt{Hz}$ S_{vd} @ 10kHz. The drain to source bias V_{ds} was -0.1V and the bulk to source bias V_{bs} was 0V.

The typical drain current vs. gate voltage characteristic (I_d-V_g) is shown in the inset of fig. 1. The threshold voltage of the device is -0.25V. The gate voltage referred noise spectrum exhibits 1/f behavior across the measured gate bias range (see fig. 1).

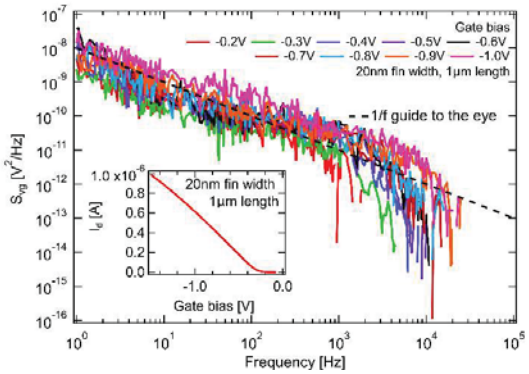

Fig. 1. Gate voltage referred noise power spectrum showing 1/f noise. A pMOS with 20nm fin width and 1µm channel length is shown. I_d-V_g of the device is shown in the inset (V_T=-0.25V).

We have investigated the geometry dependence of the gate voltage referred noise power and find the noise power to scale inversely proportional to channel length (L), as expected. The device-to-device variability in noise power was too large to assess any trends due to fin width (W) which had a limited range of 20-40nm. The noise power is expected to scale inversely with effective fin width. In terms of effective fin width (W+2H) the range was 80-100nm. See figures 2 and 3 for the geometry dependence of noise power for overdrives (V_G-V_T) of 0 and -0.5V resp.

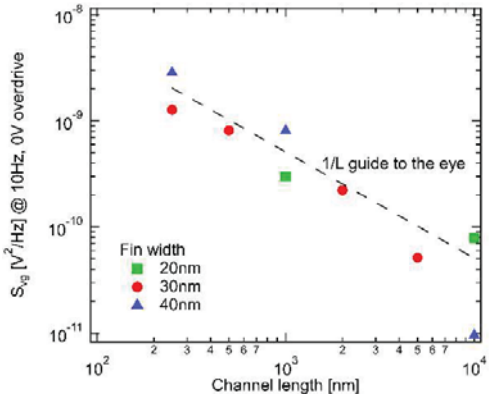

Figure 2. The channel length dependence of the gate voltage referred noise power at 0V overdrive (V_G-V_T) shows the expected 1/L scaling.

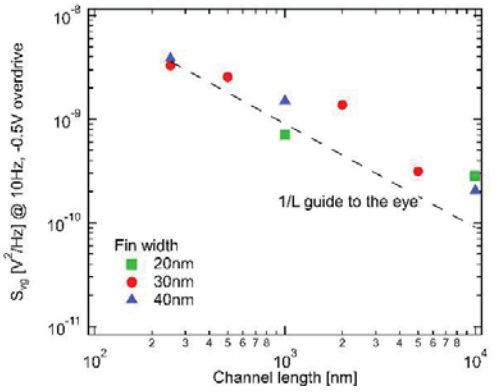

Figure 3. The channel length dependence of the gate voltage referred noise power at -0.5V overdrive (V_G-V_T) shows the expected 1/L scaling.

The gate bias dependence of the gate voltage referred noise power at 10Hz is shown in fig. 4 for 20nm finFET devices with length 1µm and 10µm. We observed that the noise power decreases with decreasing overdrive. This is in agreement with the findings of Kim et al. [2] who reported the noise characteristics of 50nm wide top-down fabricated electrolytically gated nFETs, and who also observed increasing gate bias referred noise power at higher overdrive. This is also in agreement with the carbon nanotube work [4] and the theory in [5]. Rajan et al. [3], however, reported a different gate bias dependence of noise power for 100nm wide top-down nMOSs.

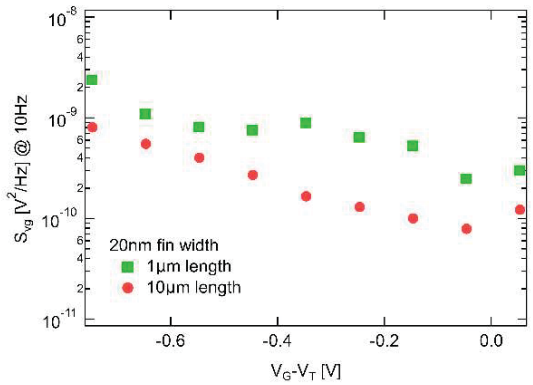

Fig. 4. Gate bias dependence of the gate bias referred noise power at 10Hz vs. overdrive for a 20nm wide finfet (gate lengths of 1 and 10µm).

We found the gate bias dependence of the noise power of the fabricated electrolytically gated FETs to be consistent with the description of number fluctuation noise with correlated mobility according to Hung et al. [5]. The gate voltage referred noise power (S_{vg}) increased quadratically below the threshold voltage with gate bias. In figure 5 the square root of S_{vg} is plotted vs gate bias and shows a linear dependence on gate bias below threshold. This behavior has also been observed for electrolytically gated FETs by Kim et al. [2]. The gate referred noise power below pMOS V_T is described by the following formula according to the number fluctuation model with correlated mobility fluctuations [5]:

$$S_{Vg} = \frac{kTq^2}{\gamma f W L C_{ox}^2}(1 + \alpha\mu N)^2 N_t$$

k is Boltzman's constant, T is temperature, q is elementary charge, γ is the attenuation coefficient of the carrier wave function in the oxide, C_{ox} is oxide capacitance, α is the scattering coefficient, μ is the mobility, N is mobile carrier charge density, and N_t is trap density.

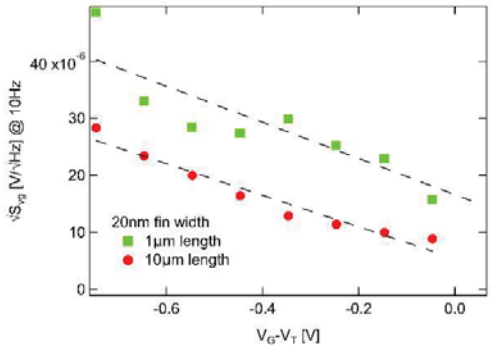

Figure 5. The square root of the gate referred noise power approximately shows a linear dependence on overdrive (V_G-V_T) below V_T in agreement with the carrier fluctuation model by Hung et al [5].

Here we report gate bias referred noise powers down to $1\times10^{-10}V^2$/Hz at 10Hz for a 20nm wide 10µm long single fin device. The gate bias referred noise PSD reported by Kim et al. [2] is significantly higher ($1\times10^{-8}V^2$/Hz) at 10Hz for a much larger device with an effective width of (50nm+2×40nm)×10 fins and a 10µm length. Converting Kim et al.'s figure to the 10µm length and 20nm+2×30nm effective width geometry reported in this work would amount to ~$1.6\times10^{-7}V^2$/Hz. Rajan et al.[3] report a minimum noise power of ~$1\times10^{-9}V^2$/Hz (already converted to the frequency and 10µm geometry reported in this work).

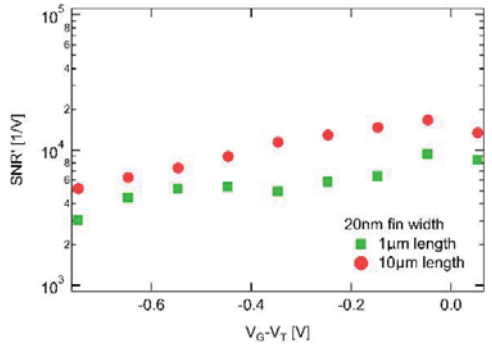

Figure 6. Square rooted inverse gate referred noise power (SNR') increases for lower overdrive voltages.

The bias dependence of the noise power determines the bias at which the signal-to-noise ratio (SNR) becomes optimal. The signal-to-noise ratio was investigated in this work for threshold shift signals (as in e.g. ISFETs) by making use of the square rooted inverse gate referred noise power as figure-of-merit for SNR:

$$\text{SNR'} = \frac{g_m[A/V]}{\sqrt{\int_{1H}^{100Hz} S_{id}[A^2/Hz]df}} = \frac{1}{\sqrt{\int_{1Hz}^{100Hz} S_{vg}[V^2/Hz]df}}$$

in which S_{id} is the drain current referred noise power spectral density and g_m is the transconductance.

We found this SNR' figure-of-merit (see figure 6) to increase for lower overdrive in contrast to the findings of Rajan et al. [3] who reported an optimum at maximum transconductance and we found the SNR' to be in agreement with the findings of Heller et al. [4] for carbon nanotube electrolytically gated FETs.

In this work we report on the noise characteristics of nanoscale top down fabricated electrolytically gated FETs with fin widths down to 20nm. We found the expected 1/f low frequency noise spectrum and noise power length scaling behavior. For a 20nm wide, 10μm long device gate referred noise power down to ~$1x10^{-10}V^2$/Hz at 10Hz was observed, which is significantly lower than previously reported for electrolytically gated top-down fabricated FETs. We find the gate referred noise power to increase with increasing overdrive, indicating the SNR to be optimal for threshold shift signals for the lowest overdrives. We have also found the dependence of gate referred noise power to be in agreement with a number fluctuation model with correlated mobility fluctuations.

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