Networks on Chips: from Research to Products

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Relentless Growth in System Performance

Moore's Law - 2005

Source: Intel
Increasing On-Chip Parallelism
Intel’s Products for Servers

Nehalem (45nm)

Westmere (32nm)
How Did Interconnects Evolve?

- Evolution to more bandwidth, more usable bandwidth
- Natural evolutionary trajectory
Interconnection Issues Today

- Timing Closure
- Routing
- Propagation Delays
- Heterogeneity
- Scalability
- Power
- (Performance) Verification
Evolving to Network-on-Chips (NoCs)
Why NoCs?

- Next step in on-going evolution

- Advantages as seen in large-area networks:
  - Scalable to many actors
  - Scalable to comparatively long distances
  - Suitable for homogeneous and heterogeneous systems
  - Well-understood theory and implementation

- Key principles:
  - Separate computation and communication concerns
  - Packet-based communication
  - Adjusted to on-chip medium peculiarities (area, power, bandwidth, latency)
The Birth of the NoC Idea

- **Architecture:**
  - Dally et al.
    - Parallel computing and wormhole routing
  - Greiner et al.
    - SPIN, the first NoC realization
  - Agarwal et al.
    - RAW architecture

- **Design Automation:**
  - Benini et al.
    - The NoC Manifesto and the first NoC synthesis tool
  - Carloni et al.
    - Separating computation and communication with latency-insensitive design
  - Goossens et al.
    - Æthereal: Support of QoS in NoCs
NoC-Based Chip Implementations

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CEA-LETI 07-10

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From Research to Products

- **Intel Polaris**
  - 2007, 80-core
  - 8x10 mesh NoC, ~365 GB/s aggr. @ 5.7 GHz
  - RESEARCH

- **Intel Single-Chip Cloud Computer**
  - 2009, 48-core, x86
  - 6x4 mesh NoC, 256 GB/s bisection
  - RESEARCH

- **Intel “Knights Corner”**
  - 2011, 50-core, x86
  - PRODUCT
Industry Traction

- Large semiconductor vendors
  - Intel: multicore x86
  - STMicro: STNoC for SoCs
  - NXP: Æthereal (now w/Virage/Synopsys)
  - Research efforts by many other players

- IP vendors
  - ARM’s AMBA 3 and 4
  - Sonics
  - Arteris
  - Silistix
  - NoCs in use today in products by TI, Toshiba, …

- Specialized product vendors
  - Tilera, Recore, …
The NoC Framework

- Software Services
  - Mapping, QoS, middleware...

- Architecture / IP
  - Packetizing, buffering, flow control...

- Physical Implementation
  - Synchronization, wires, power...

EDA Tools

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Software Services

- NoC monitoring
  - Performance
  - Faults
  - Thermal management
  - Debug traces (Goossens 08-10)

- NoC configuration
  - Performance
  - Power management
  - Security (Fiorin 08)
  - Fault management

- NoC kernel driver / middleware (Coppola)
Architecture / IP

- Basic library of NoC RTL
  - Switches (routers)
  - Network Interfaces
  - Links
- More advanced functionality available
  - Firewalls
  - Frequency converters
  - Width converters
  - Memory schedulers
  - Off-chip interfaces
  - Debugging/verification probes
Network Interfaces

- Interface core protocol with NoC
- Packeting/unpacketting
- Programmability
- Control-intensive
Switches

- Routing
- Buffering
- QoS / prioritization
- Mostly datapath
Links

- Wire segmentation by **topology design**
  - Put more switches, closer
  - Adds a lot of overhead

- Wire segmentation by **repeater insertion**
  - Flops/relay stations to break links - cheaper
  - However, repeaters still impact performance
A Complete NoC Instantiation
Physical Implementation

- Timing
  - Synchronous – multi clock
  - Mesochronous
  - Asynchronous
  - GALS

- Link design
  - LVDS, repeaters

- Fault tolerance
  - Coding
  - Redundancy
  - Retransmission

- Variability tolerance
EDA Tools

- Need for cohesive EDA flow
- Objectives:
  - Faster design time
  - Better Quality of Results
NoC Synthesis Flow

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New Frontiers

- NoCs for 3D chips
- Optical NoCs
Summary

- NoCs: from an idea to presence in products
  - Evolution of bus-based architectures
  - Streamlined, effective means of communication

- NoCs address some of the hard problems in very large chip design (Both ASIC and FPGAs)
  - Fewer design starts for large ASICs
  - Growing market of complex FPGA implementations

- NoC design is complex
  - NoC design must be supported by IP, tools and flows
  - Evolving market for EDA and key opportunity
Everything is connected!

Thank you