A 4-Terminal Method for Oxide and Semiconductor Trap Characterization in FDSOI MOSFETs

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***Abstract*—In this work, we present an experimental method that allows for a proper distinction between oxide (front or back) and semiconductor traps in FDSOI MOSFETs, using all four bias terminals. To this end, two cases of Random Telegraph Noise (RTN) measured signals are studied. It is shown that this method can also be used to localize the trap across the channel. Furthermore, the trap's electrostatic impact is proven to be misleading when it comes to trap localization in nanoscale devices.**

Keywords—Random Telegraph Noise, FDSOI, MOSFET, Characterization, Traps;

I. Introduction

Random Telegraph Noise (RTN) fluctuations [1], related to discrete traps that cause strong conductance modulation, have become very important in nano-scale devices, because their amplitude increases with surface reduction [1]. In Fully Depleted Silicon-On-Insulator (FDSOI) MOSFETs [2] in particular, apart from the fact that the traps may lay inside the bottom interface oxide, it has been suggested that RTN signals may also be related to traps in the silicon film [3],[4]. Recently, Marquez et al. [5] presented a RTN characterization method to help localize an oxide trap both vertically (in depth) and laterally (across the channel length), using all four bias terminals (front gate, bottom gate, drain and source). In this paper, we extend this method by combining front (FG) and back gate (BG) bias modes, to achieve the detection of both oxide (front/bottom) and silicon traps that can induce RTN, as well as their localization vertically and laterally.

II. RTN Amplitude and Kinetics

In order to study the behavior of RTN, there are three main parameters that should be first extracted from the time domain series and histogram, i.e. the higher current level duration, lower current level duration, and switching amplitude. Fig. 1(a) shows a typical RTN signal with two current levels in its time domain. The duration of the high current level is called capture time, τ_c, meaning the time required for the carrier to be captured into the trap. On the other side, the period of low current level is called emission time, τ_e. All these time values are extracted from the time domain through a pulse fitting process in order to calculate the mean capture, $\bar{\tau}_c$, and emission, $\bar{\tau}_e$, time constants.

The carrier capture and emission process by a trap can be defined by the Shockley-Read-Hall theory [6], [7]. First, the average capture time $\bar{\tau}_c$ for an electron in the inversion layer is given by:

$$\bar{\tau}_c = \frac{1}{\sigma n_s v_{th}} \ (a) \quad , \quad \bar{\tau}_e = \frac{1}{\sigma n_t v_{th}} \ (b) \tag{1}$$

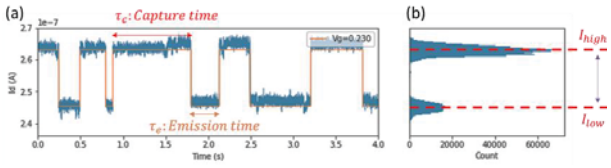

Fig. 1. Typical RTN signal: the time domain of drain current fluctuation with fitting pulse (a) and the corresponding histogram (b).

In (1), n_s is the carrier concentration near the trap in cm^{-3}, n_t is the surface carrier concentration when the Fermi level E_f crosses the trap energy E_t, v_{th} is the thermal velocity for electrons, and σ is the trap cross-section [6], [8]. For oxide traps near the interface, and considering constant mobility and drain-source voltage, n_s is proportional to the drain current, I_d, which increases with the front gate bias V_g or back bias V_b, thus $\bar{\tau}_c$ is inversely proportional to I_d. On the other hand, the trap energy level is modulated by gate voltage bias, affecting by turn $\bar{\tau}_e$ through n_t [1].

In the histogram of Fig. 1, there are two main peaks indicating I_{high} and I_{low}. The difference between the two current levels is defined as ΔI_d, describing the average amplitude of the RTN fluctuation. When a single electron with charge q is trapped into the gate oxide, it produces a local change of the flat band voltage [9]. The corresponding model predicts the RTN amplitude through:

$$\frac{\Delta I_d}{I_d} = \frac{g_m}{I_d}\frac{q}{WLC_{ox}}\left(1 - \frac{x_t}{t_{ox}}\right) \tag{2}$$

where g_m is the transconductance, W and L are the width and length of channel of MOSFET, C_{ox} is the capacitance of gate oxide per unit area, x_t is the depth of trap from the Si/SiO_2 interface, and t_{ox} is the thickness of oxide layer. In principle, (2) can be applied for both the ohmic and non-ohmic regions, demonstrating that the RTN amplitude will vary with the transistor gain, g_m/I_d. As we demonstrate in the next section, however, this approach can be misleading.

III. Results and Discussion

The devices were issued from a 14 nm FDSOI technology [2], provided by STMicroelectronics, with channel width W = 60 nm and length L = 20 nm. In total, we measured 88 dies, from which the majority had multiple RTN signals, which makes the time domain analysis complex to be processed for discrete trap parameter extraction, as needed for our study. Therefore, we chose to address two single RTN cases: a typical RTN (shown in Fig. 2(a)), in the sense that $\bar{\tau}_c$ and $\bar{\tau}_e$ change rapidly with gate bias (device #1) and a non-typical RTN (shown in Fig. 2(b)) that seemed to have a gate bias independent occupancy (device #2).

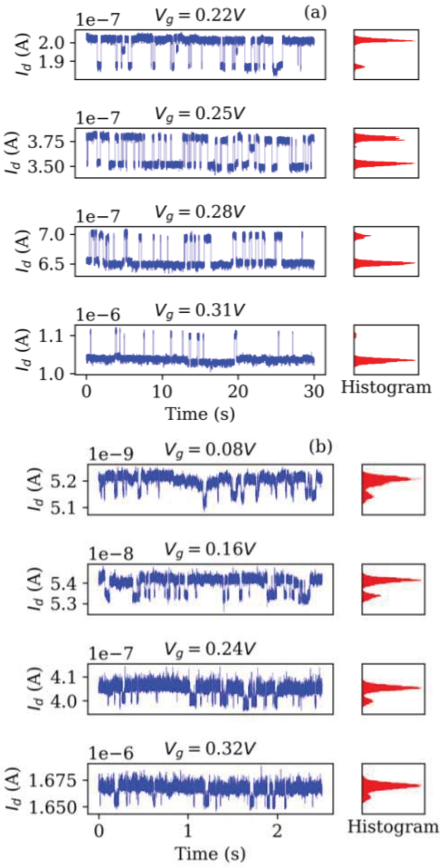

Fig. 2. The two RTN case studies: (a) typical RTN where the trap occupancy is directly affected by the gate voltage, and very rapidly and (b) non-typical RTN with a gate voltage independent occupancy.

A. *Typical RTN case (device #1)*

In Fig. 3, the relative RTN-induced drain current shift is plotted along with the g_m/I_d transistor gain, multiplied by a constant. In principle, if the two trends are similar, it means that the carrier number fluctuations (CNF) model can explain the RTN signal, through (2) [1]. However, this is in the case of classic bulk MOSFET structures, where only one silicon/oxide interface is present. In FDSOI MOSFETs, since there is a strong coupling between the two interfaces (front and back), it is not so simple to localize the trap in one of the two.

Indeed, as can be seen in Fig. 3, while we were expecting that in front gate (FG) mode, $\Delta I_d/I_d$ would be proportional to g_m/I_d, this is only true when the device is biased in back gate (BG) mode. This finding can be misleading, as one might conclude that the trap is located in the BOX (buried oxide). To further clarify the situation, we examined the drain current dependencies of $\bar{\tau}_c$ and $\bar{\tau}_e$ for both FG and BG modes.

As shown in Fig. 4, the current dependence of $\bar{\tau}_c$ is much stronger in FG mode, compared to the BG mode. In fact, the trend is very close to ~$1/I_d$. This can be explained through (1), only if the carrier density near the trap, n_s, is proportional to the drain current. The only requirement for the latter to be true is that the trap lies very close to the main channel interface. Therefore, in our case, this is a very strong indicator that the trap is inside the front oxide, not the

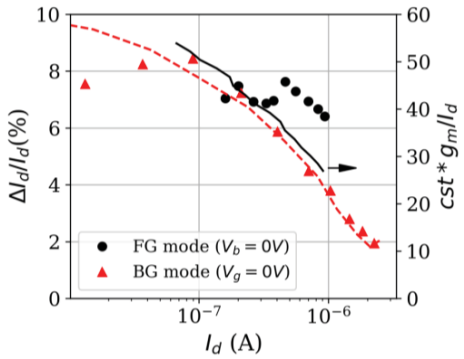

Fig. 3. Relative RTN amplitude versus drain current for front (top) and back (bottom) gate mode (case #1) under $V_d = 30$ mV.

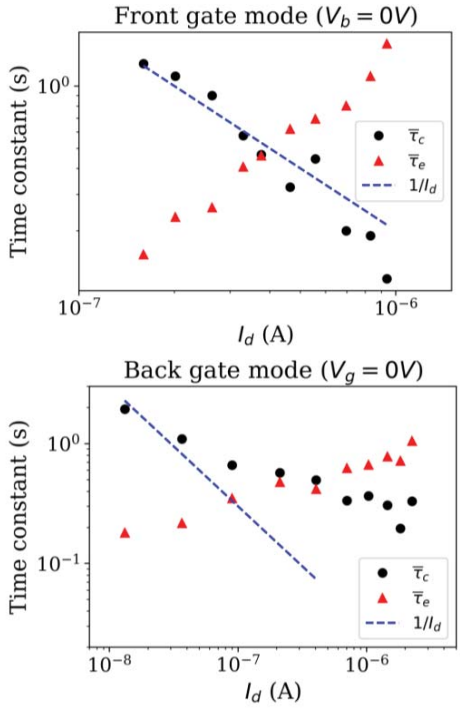

Fig. 4. Extracted capture (circles) and emission (triangles) time versus drain current under front (top) and back (bottom) gate mode for device #1 biased under $V_d = 30$ mV.

back. The small deviation from the $1/I_d$ trend can be attributed to the mobility degradation, present in higher currents. On the other side, the $\bar{\tau}_c$ - I_d dependence in BG mode is far from following the $1/I_d$ trend. This happens because the main channel is located close to the back interface, thus the carrier density at the front interface does not follow the I_d changes linearly.

Combining all the above, we can safely conclude that the RTN signal observed in device #1 is related to a trap located inside the front gate oxide. However, as noted before regarding Fig. 3, this is a surprising finding. First, it reveals that (2) in its present form cannot be used to extract the oxide trap depth in FDSOI MOSFETs. Had we followed this approach, we would have falsely located the trap in the BOX and confidently extracted x_t. Second, the FG mode trend in Fig. 3 suggests that the trapped charge gives rise to a very strong correlated mobility fluctuation, due to the very aggressively scaled gate area [10]. Third, in the opposite

case -with a RTN trap in the BOX- although $\Delta I_d/I_d$ would follow the g_m/I_d trend in FG mode, this should not lead to the conclusion that the trap is in the front oxide. Unfortunately because of this misunderstanding, there are many publications with invalid conclusions.

Concerning the trap's lateral position across the channel, one has to follow a similar procedure, by checking the amplitude and time constant dependencies on the drain-source voltage [1], [5], [11]. We biased the device varying first V_d (common source - CS) and then V_s (common drain - CD) from linear to saturation region. The corresponding extracted $\Delta I_d/I_d$ is plotted in Fig. 5, revealing a complete lack of symmetry between the two bias methods. In fact, in CD mode, the amplitude reaches a maximum of 35% (!), while in common source mode it drops very quickly from 10 to 3%, before making the RTN pulse indistinguishable.

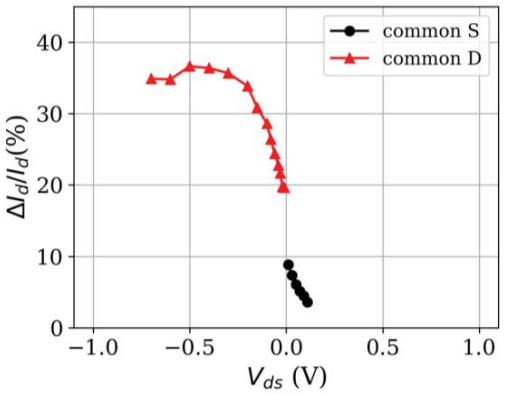

Fig. 5. Extracted relative RTN amplitude versus drain-source voltage for common source and common drain configurations (V_g = 0.25 V).

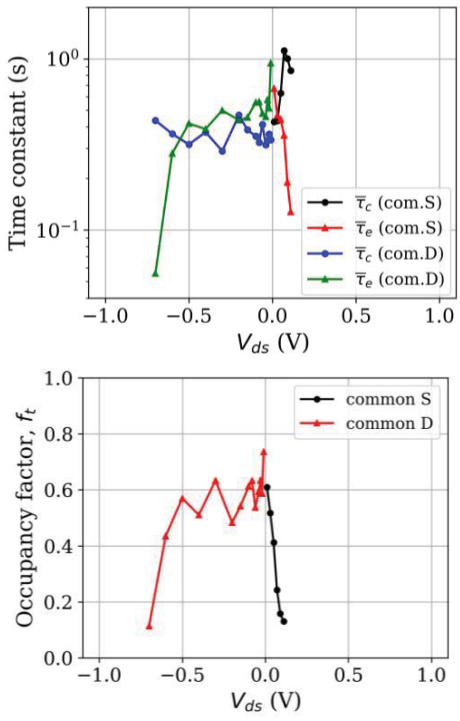

Fig. 6. Extracted time constants (top) and corresponding trap occupancy factor (bottom) versus drain-source voltage for common source and common drain configurations (device #1).

As suggested in [1] and [5], if $\Delta I_d/I_d$ increases with drain-source voltage, V_{ds}, the trap is located closer to the source. In our case, $\Delta I_d/I_d$ increases with V_{sd}, meaning that the trap lies on the side of the drain. Moreover, the sudden decrease with V_{ds}, combined with the fact that the RTN disappears after V_{ds} reaches 0.1 V (end of linear region) leads us to assume that the trap is very close to the drain/channel junction.

Once again, an assumption like this can be only verified by exploring the dependence of $\bar{\tau}_c$ and $\bar{\tau}_e$ on V_{ds}. Indeed, as shown in Fig. 6(top), $\bar{\tau}_c$ is increased suddenly in positive V_{ds} whereas $\bar{\tau}_e$ follows the opposite trend. As already pointed out, $\bar{\tau}_c$ can change only when the carrier density, n_s, near the trap is modified and $\bar{\tau}_e$ only when the trap energy level is modulated. Therefore, the sudden increase of $\bar{\tau}_c$ can be related to the carrier depopulation near the drain/channel junction, responsible for a decrease of n_s, while the decrease of $\bar{\tau}_e$ can only happen if V_d can modulate the trap energy level, which is also true for traps very close to the drain. This becomes even clearer if we plot the trap occupancy factor $f_t = \bar{\tau}_e/(\bar{\tau}_e+\bar{\tau}_c)$. As one can notice in Fig. 6(bottom), the trap maximum activity (around 55%) is only when the region near the drain is not in depletion. The decrease of f_t in high V_s values under CD mode can be regarded as a short channel effect: a source-induced barrier lowering (SIBL) near the drain. In conclusion, the initial assumption is confirmed by all the experimental results: the device #1 discrete oxide trap is next to the drain/channel junction.

B. Nontypical RTN case (device #2)

Concerning device #2, where the RTN signal behavior in terms of duty cycle seemed independent of the gate bias, as demonstrated in Fig. 2(b), we followed the exact same biasing methodology as for device #1, in order to extract all the dependencies (vs V_g, V_b, V_d, V_s) of $\Delta I_d/I_d$, $\bar{\tau}_c$ and $\bar{\tau}_e$. The corresponding results are plotted in Figs. 7-10.

First of all, $\Delta I_d/I_d$ follows the g_m/I_d trend for both FG and BG modes (Fig. 7), which initially led us to assume that it is an oxide trap. Nonetheless, in Fig. 8 we notice that $\bar{\tau}_c$ and $\bar{\tau}_e$ do not follow the $1/I_d$ trend, neither in FG nor in BG mode. On the contrary, both seem to be almost completely gate bias independent, which is an indicator for semiconductor traps [4], [10], [12]. Regarding the capture time, this means that n_s is constant near the trap and from the emission time stability it figures that the trap energy is also constant with V_g and V_b. The above can only be valid when a trap is in a depletion or accumulation region that is not affected by gate bias, which however is impossible in the channel of FDSOI MOSFETs, because of the strong front/back gate coupling. Therefore, we have to assume that the trap is located in one of the n+ doped junction regions, either source or drain.

In order to localize the semiconductor trap in one of the two regions, one has to investigate the drain-source voltage dependencies. Indeed, Fig. 9 illustrates how $\Delta I_d/I_d$ is maximized under positive source bias (CD) and how the RTN disappears for V_d>0.1V (CS), as for the trap of device #1. Nonetheless here, $\bar{\tau}_c$ and $\bar{\tau}_e$ (Fig. 10) remain constant with V_{ds} for both CD and CS modes, meaning that neither n_s nor E_t are affected. The n_s invariance confirms that the trap is located in the junction regions, where the doping prevails

over any carrier density modulations occurring in the channel.

Therefore, the device #2 semiconductor trap is with certainty localized inside the drain/channel junction. The only reason the RTN disappears above $V_d = 0.1V$ (in CS) is the pinch-off effect which results in a longer distance between the trap and the main channel, leading to a negligible electrostatic impact.

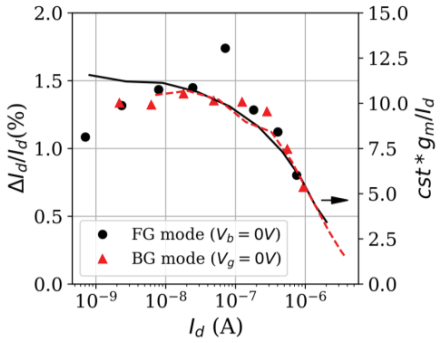

Fig. 7. Extracted relative RTN amplitude versus drain-source voltage for common source and common drain configurations.

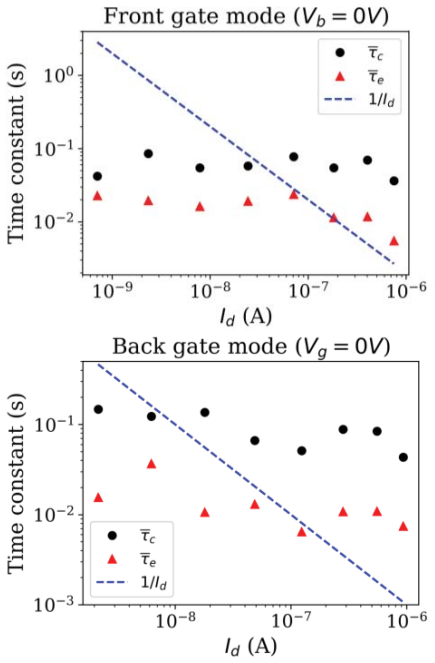

Fig. 8. Extracted capture (circles) and emission (triangles) time versus drain current under front (top) and back (bottom) gate mode for device #2.

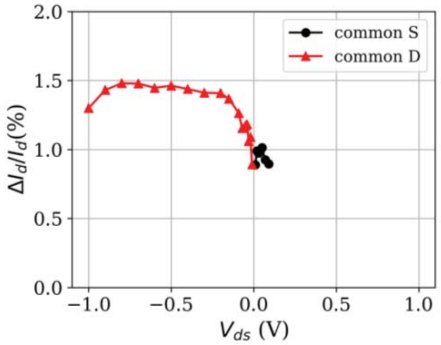

Fig. 9. Extracted relative RTN amplitude versus drain-source voltage for common source and common drain configurations.

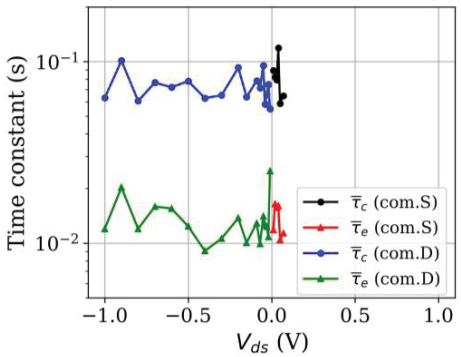

Fig. 10. Extracted time constants versus drain-source voltage for common source and common drain configurations (device #1).

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