Technologies and Platforms for Cyberphysical Systems

Giovanni De Micheli
Outline

- **Introduction**
- **Technological innovations**
  - Emerging nanotechnologies and devices
- **Architectural trends**
  - Multiprocessing, NoCs, and 3D integration
- **Cyberphysical applications**
  - The nano-tera.ch program
- **Conclusions**
Emerging societal and economic issues

- Strengthening welfare
  - Better, affordable health care and wellness
  - Dealing with ageing and young population

- Mitigating risks
  - Preventing catastrophes and pandemics
  - Monitoring the environment

- Ensuring sustainability
  - Smart energy production and distribution
  - Intelligent water management

- Enhancing security
  - Smart zero-emission data-center design
  - Preventing cyber and physical attacks

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Cyberphysical systems

[Courtesy: J. Rabaey] (c) Giovanni De Micheli
The sensory interface

- The *More than Moore* revolution

[Courtesy: ST]  [Courtesy: Carrara EPFL]

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The emerging nano-technologies

- System technology is build bottom-up, starting from materials and their properties
- New devices exploit functional geometries at the molecular level
  - Quantum confinement
- There is a plethora of new materials and processing steps/flows
  - More than 50 elements in a regular CMOS process
- *Enhanced* silicon CMOS is likely to remain the main manufacturing process
22 nm Tri-Gate Transistors

32 nm Planar Transistors

22 nm Tri-Gate Transistors

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[Courtesy: M. Bohr]
Beyond CMOS

- Nano-technology provides us with new devices
- Can they mix and match with standard CMOS technology?
- What is the added value?

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FinFETs versus SiNW FETs

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Double Independent gate SiNW FET

- Program the transistor to either p-type or n-type
Silicon Nanowire Transistors

- Gate all around transistors
- Double gate to control polarity
Device $I_d/V_{cg}$

[Courtesy: De Marchi, IEDM 12 EPFL]
Logic level abstraction

- Three terminal transistors are switches
  - A loaded transistor is an inverter
- Controllable-polarity transistors compare two values
  - A loaded transistor is an exclusive or (EXOR)
- The intrinsic higher computational expressiveness leads to more efficient data-path design
- The larger number of terminals must be compensated by smart wiring
New Design Paradigm: Ambipolar Logic

- CMOS complementary logic efficient only for negative-unate functions (INV, NAND, NOR…etc)
- Ambipolar logic is efficient for both unate and binate functions
- Optimal for XOR and XNOR dominated circuits

<table>
<thead>
<tr>
<th>Negative Unate functions</th>
<th>Binate functions</th>
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<tbody>
<tr>
<td>INV</td>
<td>XOR2</td>
</tr>
<tr>
<td>NAND2</td>
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</table>

Similar to regular CMOS

Only 4 transistors when compared to 8 transistors with a regular CMOS

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[Courtesy: H. Ben Jamaa, ’08]
Sea-of-Tiles (SoT)

- Homogeneous array of Tiles
Dumbbell-stick diagrams

Control gates connected together

Transistor pairing

Transistor grouping

Polarity gates connected together
Layout abstraction and regularity with *Tiles*

Two transistor pairs grouped together

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[Courtesy: Bobba, DAC 12]
**Biconditional Binary Decision Diagrams**

- Binary Decision Diagrams where Shannon’s expansion is replaced by the *biconditional* expansion
  
  *Biconditional* expansion:  
  
  \[ f(x, y, \ldots, z) = (x \oplus y) f(y', y, \ldots, z) + (x \oplus y) f(y, y, \ldots, z) \]

- Each BBDD node:
  - Has two branching variables
  - Implements the *biconditional* expansion
  - Reduces to Shannon’s expansion for single-input functions
BBDD: Example \((A \bigtriangleup B)(C \bigtriangleup D)\)

\[(A \bigtriangleup B)(C \bigtriangleup D)\]:
  - if \(A = B\), then true
  - else if \(C = D\), then true
  - else false
  - else false
Efficient Direct Mapping of BBDD Nodes

- **Logic level**
  - $f(A,B,..,Z,..) = F$
  - $f(B',B,..,Z,..) = G$
  - $f(B,B,..,Z,..) = H$

- **MUX driven by a XNOR**
  - $f(A,B,..,Z,..) = F$

- **Ambipolar realization**
  - $A' \oplus B$

- **Transistor level**
  - $A \oplus B$
  - $A + B$
  - $A' \oplus B$

- **CMOS realization**
  - $A \oplus B$
  - $A + B$
BBDDs are Compact (Adder Function)

Number of nodes of adder(n):
3n + 1
BBDDs are Compact (Majority Function)

Number of nodes of $\text{MAJ}(n)$:
\[
\frac{1}{8}n^2 + \frac{1}{2}n + \frac{11}{8}
\]

$\text{MAJ}(3)$: 4
$\text{MAJ}(5)$: 7
$\text{MAJ}(7)$: 11

....
Summary – technological innovations

- New materials and new device geometries
  - Silicon FIN-FETs and NanoWires
- New-properties
  - Controlled polarity transistors
- Design opportunities
  - More efficient design of data paths and computational units
  - Higher computational density

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System architectural trends

- Move towards many-core
  - Frequency scaling has leveled-off
  - Exploit application-level parallelism

- On-chip communication
  - Bottleneck for system performance

- Networks-on-Chip (NoC)
  - Adopted as scalable interconnect
  - [Benini & De Micheli 2002]

Intel Single-Chip Cloud Computer

[Courtesy: Hoçward, ISSCC 2010]
Networks-on-Chip Scalable Interconnect

- NoC modular architecture
  - Network Interfaces (NIs)
  - Switches
  - Links

- Scalable
  - Multiple parallel transactions
  - Segmented point-to-point wires

- Used in prototypes and products
  - Intel Polaris, SCC, Bone
  - TI OMAP, Tilera TILE-Gx

[courtesy: Stergiou DATE 2005]

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Specialization for Power Efficiency

- Limited power budget for mobile applications
- Trade-off programmability for power-efficiency
- Specialized heterogeneous IP-cores

- Communication is a major power consumer
  - Traffic patterns are known
  - Application specific NoC design is needed

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Application specific NoCs

- **Challenges**
  - Many parameters (i.e., data-size, frequency, connectivity)
  - Tools are required to find the best topology

- **New technologies**
  - More IP-cores
  - More constraints (i.e., 3D-IC vertical connectivity)

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Design automation for NoCs

- Large design space
  - What topology?
  - Which mapping?
  - Which routes to use?
- Optimize parameters
  - Link width, buffer sizes
- Simulate, verify, test
Three Dimensional Integration

- System in Package
  - Better form factor
  - Limited vertical connectivity

- Monolithic Integration
  - New experimental process (LETI)
  - New use of RRAMs in BEOL

- Stacking with Through Silicon Vias
  - Reduce average length of on-chip global wires
  - Increase performance
    - Processor/memory systems – Wide I/O
  - Heterogeneous integration

[E. Beyne ITC 06]
3D NoC Design

- Use NoCs to support Wide I/O
- Challenges:
  - Meet application constraints in a 3D structure
    - Bandwidth, latency
    - Which topology, switches, layers and floorplan locations?
  - Meet 3D technology constraints
    - Maximum available TSV constraints
    - Communication between adjacent layers

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Extending 3D Integration to sensing

Custom micro-fabrication for the bio-layer

Technologies enabling low noise operation for the analog circuits

High speed/density CMOS technologies for digital circuits and memories

[ Courtesy Guiducci: 2010]
Disposable bio-layer

- No need for cleaning. Bio-layer is disposed after each measurement and CMOS layers are used repeatedly

- Increased sensitivity and array density due to vertical interconnections from the bio-layer to the readout electronics

- Sophisticated algorithms for highly-specific target identification run on-chip DSP and memory

[ C. Guiducci 2010]
Memristive SiNW-based Biosensors

- Crystalline, free-standing, Silicon Nanowires manifest memristive conductivity due to the nano-scale of the fabricated structures.
- The voltage-gap between the forward and backward current minima in I/V curves increases after NW functionalization with antibodies.

In a controlled humidity range, Si NW device sense antigen molecules (i.e., cancer biomarkers) thanks to molecule up-take (immuno-recognition events) displayed by voltage gap changes.

CVD-MWCNTs for electrochemical biodevices

Objective

MWCNTs directly grown by CVD onto Pt microelectrode-array to enhance sensing performance of electrochemical biodevices

1. Microfabricated biosensor
2. Iron catalyst nanoparticles electrodeposition
3. CVD-MWCNTs grown onto working electrodes
4. Electrochemical detection of a biocompound by using Pt electrodes nanostructured with CVD-MWCNTs
Integrated sensing platforms

- Specific components
  - Probes and electrodes
  - Chambers and fluidic circuits

- Electronic components
  - Transconductance amplifier and data conversion
  - Transmission and powering
Summary – architectural trends

- Multi-processing *component-based* design paradigm
- Networks on Chip to address communication challenge
  - Adopted by virtually all manufacturing companies
  - Different flavors to address different application domains
- 3-Dimensional integration
  - Lower latency in multiprocessing system
  - Enabler of heterogeneous integration
- Hybridization of technologies
  - Support for integrated sensing and processing
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Mission

Research, Design & Engineering of complex tera-scale systems using nano-scale devices and technologies

Foster research and crossbreeding of technologies

Main application domains are Health and Environment, with Energy and Security as transversal support areas

• Develop new markets
• Improve living standards
• Better the quality of health and environment
• Foster a vision of engineering with social objectives
• Promote related educationl programs
Nano-Tera.ch: key figures

- ~120 projects funded since 2009
- ~30 MCHF/year (approximatively 50% in cash + institutional matching)
- ~35 Swiss research institutions involved
- ~150 research groups
- ~700 researchers
- ~180 PhD thesis supported
- ~750 papers published
- ~1300 presentations
- ~35 awards
- ~25 patents filed

<table>
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<th>TOTAL since beginning of the program</th>
<th>Journals, books</th>
<th>Conf. Proceedings</th>
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Examples of research projects
Implanted sensor

Portable Device

Power & Data Transmitter Unit

Receiving Antenna
Power Module + Sensor
Target: Safety in an alpine environment
Technology: Networked stations for rock/ice movement
Nano-Tera.ch exploits **new technologies** and devices:
- *Integrated electronics* and *sensors*

With the objective of building **heterogeneous** systems:
- Monitor health in patients, disabled and elderly
- Monitor the environment for pollution and to prevent disasters

And with the final goal of increasing the **well-being** of individuals and communities
- Key contribution of engineering to coping with complex societal and economic problems
- Requiring large and collaborative intellectual effort

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Conclusions

- Cyberphysical systems can support the solution of important societal and economic problems
- Cyberphysical systems exploit ubiquitous connectivity and new sensing modalities
- New technologies enrich CMOS with novel devices
  - *Silicon nanowire* and *carbon-based* devices
  - *Controlled polarity* can be efficiently used in logic design
- New architectures and design styles:
  - *Regularity* of the fabric is key to robustness
  - 3-Dimensional integration gives an extra degree of freedom
- Hybridization of new technologies opens new frontiers
Thank you