LOW VOLTAGE SIC-MOSFET BASED MEDIUM VOLTAGE CONVERTER

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Switzerland
PEL RESEARCH FOCUS

MVDC Technologies and Systems
▶ System Stability
▶ Protection Coordination
▶ Power Electronic Converters

Power Electronics Conversion
▶ Multilevel Converters
▶ Solid State Transformers
▶ Medium Frequency Conversion

Components
▶ Semiconductors
▶ Magnetics
▶ Characterization

Power Density [kW/l]
0 5 10 15 20 25 30
Efficiency [%]
98.6
98.8
99
99.2
99.4
99.6
99.8
100
All Designs
Filtered designs
Designs with standard core and wire
Filtered standard designs
Selected design

ECPE Workshop, Freiburg, Germany
December 3-4, 2019
IMPEDANCE/ADMITTANCE MEASUREMENTS AT MEDIUM VOLTAGE

AD/DC distributed power system

Power electronics dominated energy system require careful design and stability studies

System identification is challenging at medium voltage level [1]
MV GRID EMULATOR FOR PHSP RT-HIL

Medium Voltage Research Platform - MV Grid Emulator is needed!
- Extending flexibility of pumped hydro storage plants
- Assessment of ancillary services
- Converter Fed Synchronous Machines - CFSM
- Doubly Fed Induction Generator - DFIG
- Novel power electronics conversion technologies [2]

- A Medium Voltage Pumped Hydro Storage Plant Emulation Platform (0.5MVA, 6kV)
- ACS2000: 1MW, 6kV, 4Q 5-level drive
- IM (left) + SM (right): 0.5MVA, 6kV, 4p, 1500rpm

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**Table 1**  Grid Emulator Parameters

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<tr>
<th>Parameter</th>
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<td>1 MVA</td>
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<tr>
<td>transformer primary side line voltage</td>
<td>6 kV</td>
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<td>transformer secondary side line voltage</td>
<td>710 V</td>
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<tr>
<td>maximum cell dc link voltage</td>
<td>1200 V</td>
</tr>
<tr>
<td>CHB output line voltage</td>
<td>0 to 6 kV ac or ±5 kV dc</td>
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One goal is to avoid need for these filters!

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Another goal is to achieve high control bandwidth at the output!

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MEDIUM VOLTAGE GRID EMULATOR - 4Q ROBICON TOPOLOGY

▲ CHB topology with 15 LV cells and (small) output filter

▲ Bidirectional CHB cell without input filter and with SiC output stage

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MULTIWINDING PHASE-SHIFT TRANSFORMER

- 1MVA rated
- 6kV primary winding
- 15 x 710V secondary windings
- Complex but relatively cheap
- Not a symmetrical structure [3]
- Turns ratio and phase deviations

▲ 1MVA, 6kV multiwinding transformer

▲ Detailed and accurate PLECS simulation model is available

▲ Measured and simulated short circuit impedances
GRID SYNCHRONIZATION - PLL VOLTAGE SENSING LOCATION?

▲ Multiple secondary side PLLs

▶ Transformer secondary winding voltage as source
▶ Local PLL on each cell
▶ Transformer parameters mismatch not relevant
▶ Discrete filters are needed in front of the AFE - bulky!
▶ Straightforward solution

▲ Single primary side PLL

▶ Grid voltage as source
▶ Transformer leakage inductances used as filter
▶ Transformer nameplate parameters used (ratio, phase)
▶ No discrete filters are needed in front of the AFE - savings!
▶ Preferred solution [4]
CONTROL IMPLEMENTATION

▲ Multiple secondary side PLLs

▲ Single primary side PLL

▲ SRF PLL is used for both cases

▲ AFE input current controller in SRF

▲ AFE DC link voltage controller

▶ PR controllers in SRF for AFE input current control
▶ PI DC link voltage controller
▶ CHB operation causes 2nd harmonic ripple
▶ Notch filter on measured DC link voltage
▶ PSC PWM
▶ Controller parameters are available in [4]
SIMULATION RESULTS...

▲ Multiple secondary side PLLs

▲ Single primary side PLL

▲ Performances during load change - with discrete filters and multiple PLLs on the secondary side

▲ Performances during load change - without discrete filters and with single PLLs on the primary side
SIMULATION RESULTS

PLL Output: Phase Angles
PLL Output: Amplitudes
Difference between PLL Phase Angles and Grid Phase Angle

PLL performances: primary side based (black) and secondary side based (colored)

Grid side current spectrum

AFE current waveforms
SEMICONDUCTOR CONSIDERATIONS?

▲ Static characteristic of several considered modules

▲ Switching energies at 1200 V

<table>
<thead>
<tr>
<th>Halfbridge Module</th>
<th>Short Designator</th>
<th>Package</th>
<th>$T_{j,SW}$ ($\degree$C)</th>
<th>$T_{j,D}$ ($\degree$C)</th>
<th>$R_{g,on}$ (Ω)</th>
<th>$R_{g,off}$ (Ω)</th>
<th>Ref.</th>
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<tr>
<td>CAS300M17BM2</td>
<td>SiC I</td>
<td>62 mm</td>
<td>150 $\degree$C</td>
<td>150 $\degree$C</td>
<td>2.5 Ω</td>
<td>2.5 Ω</td>
<td>[5]</td>
</tr>
<tr>
<td>APTMC170AM30CT1AG</td>
<td>SiC II</td>
<td>SP1</td>
<td>150 $\degree$C</td>
<td>175 $\degree$C</td>
<td>10 Ω</td>
<td>10 Ω</td>
<td>[6]</td>
</tr>
<tr>
<td>2M1400VE-170-53</td>
<td>Hybrid</td>
<td>M277</td>
<td>150 $\degree$C</td>
<td>150 $\degree$C</td>
<td>1 Ω</td>
<td>0.5 Ω</td>
<td>[7]</td>
</tr>
<tr>
<td>SKM150GB17E4</td>
<td>Si IGBT</td>
<td>34 mm</td>
<td>150 $\degree$C</td>
<td>150 $\degree$C</td>
<td>2 Ω</td>
<td>2 Ω</td>
<td>[8]</td>
</tr>
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</table>
SEMICONDUCTOR LOSSES

\( \Delta \) AFE losses per switch, \( P = 1 \text{ MW} \).

\( \Delta \) Inverter losses per switch, \( P = 1 \text{ MW} \).
SEMICONDUCTOR LOSSES...

▲ 4Q cell losses for different $f_{SW}$ with same modules in both stages

► Full SiC - nice, efficient, but not critical for AFE
► Hybrid solution seems more appropriate and cost effective
► AFE 10 kHz (Si) + CHB 20kHz (SiC)

▲ 4Q cell semiconductor efficiency for switching frequency ranges
Three-phase supplied Active Front End (AFE) interfaced to single phase inverter with an LC filter.

- AFE regulates DC link voltage
- Slower dynamics of AFE
- Impact on the CHB output?
- Source affected impedance
- Need to characterize source impedance?

- HB inverter with an LC filter
- HB inverter with an LC filter and internal $Z_{source}$
Three-phase AFE feeding a load.

Output, dc side, impedance of the AFE under the input current and output voltage control loops closed.

Hardware in the loop system

- RT-Box based HIL
- Power hardware emulation
- Control on the DSP
- PRBS injection
- High flexibility in work
Closed-loop dynamics of the HB inverter with cascaded inductor current and capacitor voltage control.

Comparison of control-to-output $G_{cvc}$ characteristics of a HB operating with an ideal dc link voltage and with AFE as an input stage controlling the dc-link voltage.

$d$-axis control-to-output characteristics $G_{cvc,cl,dd}$ of the HB-inverter supplied from ideal DC source.

$d$-axis control-to-output characteristics $G_{cvc,cl,dd}$ of the HB-inverter operated with AFE as the input stage.
ONGOING HW DESIGN

- 1.7kV Si IGBT (62mm package)
- 1.7kV SiC MOSFET (samples from Mitsubishi Electric)
- Cost design optimization of HW
- ABB AC 800PEC as main controller
- Communication, measurements, protection
- Mechanical design...

▲ 4Q PEBB under testing (communication)
▲ 4Q PEBB - present design
SUMMARY

- 4Q Robicon based Grid Emulator
- Hybrid design: AFE (Si), CHB (SiC)
- Perturbation Injection Converter for system identification
- Primary side PLL allow for significant cost savings
- Robust control despite transformer asymmetries
- SiC devices enabling high output control bandwidth!

▲ 1MVA, 6kV multiwinding transformer

Secondary Side Terminals:
- Group A1 to A5
- Group B1 to B5
- Group C5 to C1

▲ SiC PEBB during gate driver testing
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