# Low frequency noise characterization and modeling of SiGe HBT featuring LASER annealing in a 55-nm CMOS node

J.El Beyrouthy, A. Vauthelin, B. Sagnes, F. Pascal, A. Hoffman, M. Valenza
IES, Univ Montpellier, CNRS
Montpellier, France
bruno.sagnes@ies.univ-montp2.fr

S. Haendler, A. Gauthier, P. Chevalier, D. Gloria
STMicroelectronics, 850 rue Jean Monnet
38926 Crolles Cedex, France

***Abstract*— This work presents Low Frequency Noise (LFNoise) characterization and modeling performed on DPSA-SEG SiGe HBT integrated in a 55-nm CMOS node. The aim of this study is to evaluate the advantage brought by the implementation of a Dynamic Surface Annealing (DSA) in addition to the well-known Spike Annealing process.**

**The HBTs are supplied by STMicroelectronics Crolles and present transit ($f_T$) and maximum oscillation ($f_{MAX}$) frequencies in the 320-370 GHz range.**

**Spectra can be affected by the presence of generation-recombination (GR) components. The 1/f noise amplitude is modeled following the SPICE compact model, and the 1/f parameters $K_F$ and $A_F$ are calculated. The extracted figure of merit $K_B = K_F A_e$ has a very good value of 6.8 $10^{-10}$ µm² for transistors processed using the DSA technique.**

***Keywords*— HBTs, BiCMOS technologies, Low Frequency Noise, 1/f Noise, Laser annealing**

## I. INTRODUCTION

Over the last ten years, there has been an increasing demand for RF, MMW, optoelectronics and for future TeraHz applications. In order to provide integrated circuits in such high frequency range, elementary bipolar transistors should reach very high frequency performances. If at the beginning III-V transistors seemed to be the most promising in terms of frequency performance, the Si/SiGe base-emitter Heterojunction Bipolar Transistors (HBT) appeared in the early 2000s as one of the best candidates. In addition to its excellent performances, its compatibility with conventional CMOS technologies also makes this technology essential.

The HBT devices studied in this work are developed by STMicroelectronics for RF, MMW and THz applications in the framework of the ongoing European TARANTO project [1]. They are based on the structure of reference used in the B55 technology [2] and showing 320 GHz $f_T$ and 370 GHz $f_{MAX}$ performances.

In order to achieve that objective, the HBTs process includes a Double-Polysilicon Fully-Self-Aligned architecture associated with a selective SiGe:C epitaxy for the base. In particular, to control the DC and HF transistor performances, it is essential to control the emitter-base junction doping level. For instance, to prevent the out-diffusion of Boron and thus to control the base doping profile, some carbon (< 1 %) is incorporated in the SiGe layer. Still focused on the optimization of the E-B junction, another important step process is the optimization of the thermal budget used to activate the dopants (note that effective activation of dopants is also important to lower sheet resistances). Thus, in order to improve the performance of the transistors while remaining compatible with CMOS technology, the thermal budget should be carefully adjusted.

This paper presents a comparison of low frequency noise (LFNoise) characteristics in Si/SiGe:C HBTs processed using two distinct dopants activation techniques. The first one used a classical thermal activation technique (spike annealing), referred to as B55THA, while the second one used a DSA (Dynamic Surface Annealing) process, referred to as B55DSA, in addition to a lower spike annealing temperature. This is done in order to limit the dopant diffusion while providing a higher activation level [3]. The main goal of this work is to evaluate the advantage brought by the implementation of a Dynamic Surface Annealing. DC characteristics will be compared but, due to its sensibility, a focus will be made on LFNoise (spectral analysis and 1/f noise modeling). If most of the LFNoise works on modern bipolar transistors lead to the conclusion that 1/f noise sources are located in the emitter-base region (mainly in its intrinsic part), investigations on different technological parameters are needed in order to go further [4] [5] [6]. In this frame, the comparison of HBTs developed with and without the DSA process could also be of interest.

## II. EXPERIMENTAL SETUP AND DEVICES

The measurements are performed using a manual probe station. On-wafer contacts are performed using coplanar probes. I-V characteristics (Gummel-plots) are measured using a Keithley 4200 semiconductor characterization system. LFNoise measurements are performed in the 10 Hz-100 kHz frequency range. HBTs are biased in a common emitter configuration. 3 emitter areas are studied for the B55THA process ($A_e$ = 1, 3 and 4.2 µm²), and 4 for the B55DSA one ($A_e$ = 0.6, 1, 2.5, and 4.2 µm²). For each area, measurements are performed on several dies. The input base current noise spectral density, $S_{IB}$, is measured in high impedance configuration (Figure 1), with a spectrum analyzer (HP89410A) and a low noise transimpedance amplifier (EG & G 5182). The transistors are placed in a

Faraday cage and biased by batteries to avoid external disturbances.

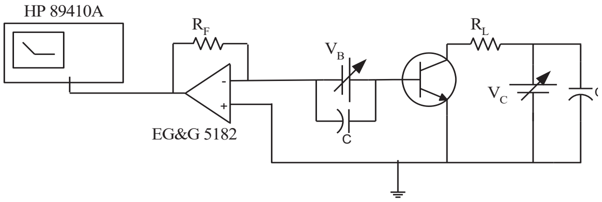

Fig.1: LFNoise experimental set-up used for the measurement of the input base current spectral density, $S_{IB}$.

## III. DC CHARACTERISTICS

Figure 2 and 3 show typical Gummel plots obtained on both B55THA and B55DSA processes. For each technology, 3 devices with an emitter area of 4.2 µm² are plotted. Same base and collector current components are observed. The die to die dispersion (measured over 10 dies) is ranging between 4 and 7%. The maximum current gain $h_{FE}$ is of 2300 and 2500 for B55THA and B55DSA transistors respectively.

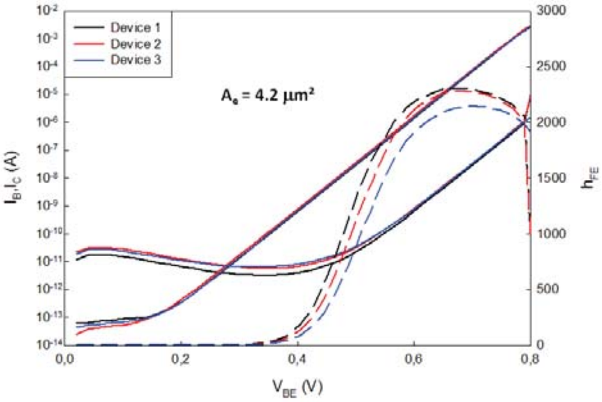

Fig.2: Gummel plot and current gain of 3 HBTs of the B55THA process, $A_e$ = 4.2 µm².

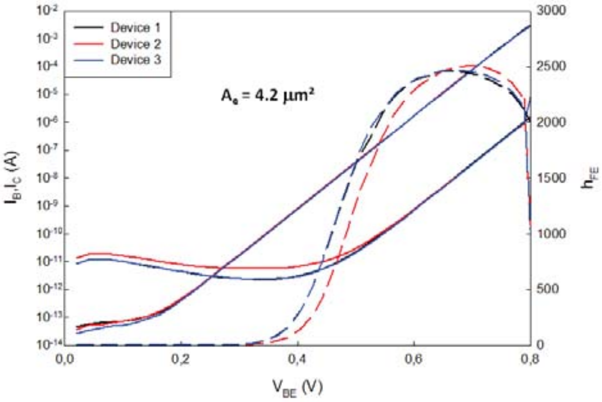

Fig.3: Gummel plot and current gain of 3 HBTs of the B55DSA process, $A_e$ = 4.2 µm².

## IV. LOW FREQUENCY NOISE CHARACTERISTICS

We measured $S_{IB}$ as a function of the base bias current and the emitter area $A_e$. Representative spectra obtained on both type of transistors are reported in Figures 4 and 5. For instance, concerning the spectra obtained on B55DSA (Figure 5), 11 HBTs with an emitter area of 1 µm² were tested. 5 exhibit spectra composed of a 1/f noise component followed by the shot noise $2qI_b$, the others are affected by the presence of generation-recombination (GR) components more or less pronounced. The 1/f noise amplitude dispersion is estimated to be less than one decade. More generally, almost 40 % of the tested components are GR free whatever the type of transistors.

As reported in [11], we found that most of the GR components are related to RTS noise. To take into account the presence of GR components, a statistical approach (i.e. average spectrum done over a large number of measured spectrums) was proposed in Poly-Emitter BJTs [7] and in SiGe HBTs [8].

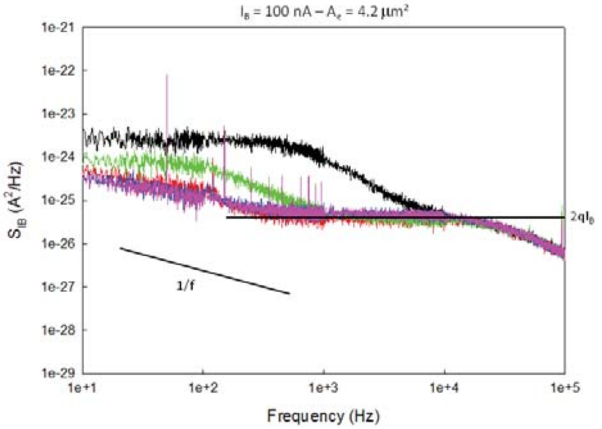

Fig. 4: Examples of spectra obtained on 6 HBTs of emitter area $A_e$ = 4.2 µm² and for $I_B$ = 100 nA (B55THA)

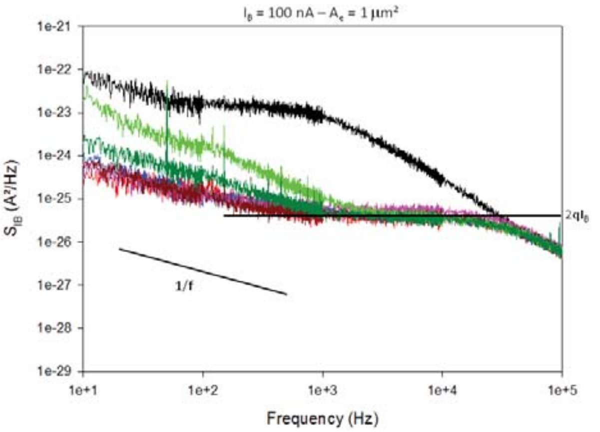

Fig. 5: Examples of Spectra obtained on 6 HBTs of emitter area $A_e$ = 1 µm² and for $I_B$ = 100 nA (B55DSA).

Now, focusing on the 1/f noise component only, its amplitude is modeled using the usual 1/f SPICE model [9] :

$$S^{1/f}{}_{IB} = K_F \frac{I_B^{A_F}}{f} \qquad (1)$$

where $K_F$ is the parameter representing the 1/f noise amplitude and $A_F$ its evolution with the base bias current.

The evolution of $S_{IB}$ at 1 Hz versus base current $I_B$ determines the $A_F$ coefficient. Figure 6 gives a representative example of $S_{IB}$ at 1 Hz versus $I_B$ for B55DSA HBTs with 3 emitter geometries. Base bias currents are 50, 100 and 500 nA. As can be seen, a quadratic dependence is found leading to a value of $A_F$ close to 2. Same behavior was observed for the B55THA process. This classic result was reported in all the works related to 1/f noise in modern Si-BJTs [10] and SiGe HBTs [5].

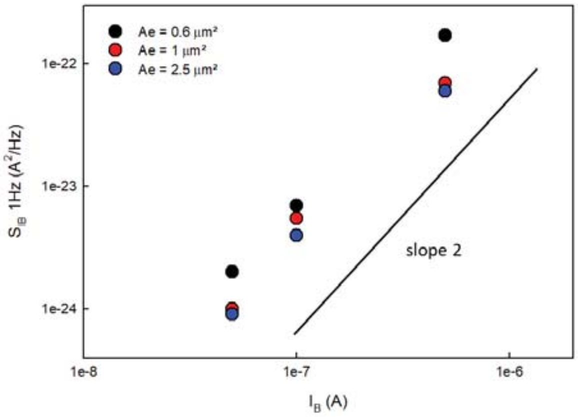

Fig. 6: B55DSA 1/f noise level ($S_{IB}$ at 1 Hz) versus the base current $I_B$.

The 1/f noise level is then studied as a function of the emitter area. In Figure 7, where the dimensionless coefficient $K_F$ is plotted versus $A_e$, for several dies, the general trend for the two types of processes is that the 1/f noise level is found to be inversely proportional to the emitter area. The 1/f noise dispersion observed in both Figures 4 and 5, for emitter areas of 4.2 and 1 µm² as examples, confirms that the dispersion is always less than one decade. Nevertheless, the mean 1/f noise level is slightly lower in the case of the DSA technique. As $K_F$ is found to be inversely proportional to $A_e$, the product $K_F$ x $A_e$ = $K_B$ (in µm²) can be used as a very convenient figure of merit in order to compare different technologies [9] [11] or processes/parameter steps [6]. The comparison between the two types of transistors is in favor of the DSA technique with a value of $K_B$ of 6.8 $10^{-10}$ µm² versus 1.3 $10^{-9}$ µm² for the THA one.

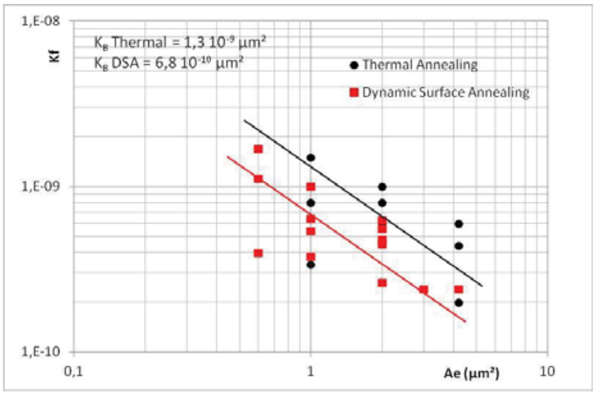

Fig. 7: SPICE parameter $K_F$ versus emitter area $A_e$

## V. DISCUSSION/CONCLUSION

The impact of the DSA process on high frequency performances results in the improvement in HBT transit frequencies of 5 – 7 % (due to a decrease of As-dopant diffusion from emitter) and in a better MOSFET compatibility [3].

From our DC characterizations, we observed an increase of the current gain $h_{FE}$ in HBTs processed with the DSA technique compared to the THA one. In both types of transistors, a small dispersion of the DC results is observed.

Concerning the focus of this work (i.e the comparison of the LFNoise of 2 types of transistors), the global behavior of LFNoise remains unchanged: GR components are always present with characteristics (cut-off frequencies and plateaus) that can vary very significantly and randomly. The 1/f noise level is reduced by a factor 2 for the B55DSA HBTs compared to the B55THA ones. Hence the reduction of the 1/f noise is noticeable. In both cases, the 1/f noise dispersion remains reasonable. The approximate $K_B$ values of 6.8 $10^{-10}$ µm² and 1.3 $10^{-9}$ µm² for DSA and THA respectively are very good even if they do not reach the very best ones of 4 $10^{-11}$ µm² [12] and 6.7 $10^{-11}$ µm² (our result) [13], both obtained from mature 130 nm BiCMOS technologies. Note that these best values are obtained from a single die, no dispersion was taking into account in ref. [12], while we published in [8] extended works (statistical study based on 61 tested devices) leading to a mean value of 6 $10^{-10}$ µm². In order to take into account the high frequency and the LFNoise performances, a better figure-of-merit was introduced: the ratio $f_c/f_T$ [14] [11]. $f_C$ is the 1/f noise corner frequency, measured from the intercept of the 1/f component and the white noise on the $S_{IB}$ spectrum. This parameter is the image of the 1/f noise amplitude. $f_T$ is the transit frequency. The use of this figure-of-merit is clearly in favor of the DSA technique as both $f_T$ and $f_C$ are improved.

Concerning the localization of the 1/f noise sources, the combined effect of the 1/f noise level ($S_{IB}$ at 1 Hz) quadratic dependence on the base current and the 1/$A_e$ dependence of $K_F$ indicates that the associated noise sources are uniformly distributed over the entire emitter area. This conclusion, which is found in all the papers concerning 1/f noise in recent bipolar transistors, is based on the study of several physical models referring to an $I_B^2$ law and an $A_e^{-1}$ dependence [9] [15]. Also, the study of the voltage coherence function (between input ($v_b$) and output ($v_c$) fluctuations), gives a direct argument concerning the localization of the 1/f noise sources at the emitter-base junction [12] [16]. Even if almost all the published work indicates that the 1/f noise sources are homogenously distributed at the emitter-base area, there is no evidence of their exact localization. This is due to the sophisticated architecture of the emitter-base region with, in addition to the complex internal junction, the possible influence of the oxide spacer, emitter perimeter, series resistance, poly-silicon/silicon interface…

Concerning the observed reduction of the 1/f noise in the DSA transistors, the question is: can it be a direct proof of the effect of this technique and thus demonstrate the better structural or electrical quality of the deposit layer (more effective activation of dopants)? Not sure because it could be an indirect effect associated to the better control of the dopants, for instance a better control of the emitter-base junction depth can play a role. Effectively we have clearly demonstrated in [17] that when the electrical E-B junction depth increases (with respect to poly/mono interface), the 1/f noise level decreases. This could be attributed to the reduction of the interaction of the minority carriers with interface states located at the poly/mono interface.

## ACKNOWLEDGMENT

This work was done in the frame of the TARANTO H2020 ECSEL project, co-funding by the French Ministry of Economy, Finance and Industry.

## REFERENCES

[1] P. Chevalier et al *"SiGe BiCMOS Current Status and Future Trends",* BCICTS, 2018, pp. 64 – 71

[2] P. Chevalier et al, "A 55nm triple gate oxide 9 metal layers SiGe BiCMOS technology featuring 320 GHz $f_T$ / 370 GHz $f_{MAX}$ HBT and High-Q Millimetter-Wave Passives", *in Proc.* IEDM, 2014, pages 77-79

[3] A. Gauthier et al "SiGe HBT / CMOS Process Thermal Budget Co-optimization in a 55-nm CMOS Node", *in Proc. BCTM*, 2017, , pages 58-61

[4] J. Raoult, et al., "Impact of carbon concentration on 1/f noise and random telegraph signal noise in SiGe:C heterojunction bipolar transistors," Journal of Applied Physics, vol. 103, pp. -, 2008.

[5] F. Pascal, et al., "Improvement of 1/f noise in advanced 0.13 µm BiCMOS SiGe: C Heterojunction Bipolar Transistors," in Noise and Fluctuations (ICNF), 2011 21st International Conference on, 2011, pp. 279-282

[6] B. Sagnes et al. "Low Frequency Noise in advanced 55nm BiCMOS SiGeC Heterojunction Bipolar Transistors : impact of collector doping", in Proc. ICNF, 2017

[7] M. Sandén, O. Marinov, M.J. Deen, M. Ostling, IEEE Transactions on Electron Devices,, 49 (2002) 514-520

[8] M. Seif, F. Pascal, B. Sagnes, A. Hoffmann, S. Haendler, P. Chevalier, D. Gloria "Dispersion study of DC and Low Frequency Noise in SiGe:C Heterojunction Bipolar Transistors used for mm-Wave to Terahertz applications " Microelectronics Reliability (2014) DOI: 10.1016/j.microrel.2014.07.027

[9] M. Deen and F. Pascal, "Review of low-frequency noise behaviour of polysilicon emitter bipolar junction transistors," in *Circuits, Devices and Systems, IEE Proceedings-*, 2004, pp. 125-137

[10] M.J. Deen ; E. Simoen "Low-frequency noise in polysilicon-emitter bipolar transistors" IEE Proceedings - Circuits, Devices and Systems,2002, pp. 40-50

[11] M. Seif, F. Pascal, B. Sagnes, J. Elbeyrouthy, A. Hoffmann et al. "Characterization, modeling and comparison of 1/f noise in Si/SiGe:C HBTs issued from three advanced BiCMOS technologies", in Proc. ICM, 2017

[12] Chhandak Mukherjee, Thomas Jacquet, Anjan Chakravorty, Thomas Zimmer, Josef Böck, Klaus Aufinger, Cristell Maneux, "Low-Frequency Noise in Advanced SiGe:C HBTs—Part I: Analysis", IEEE Transactions on Electron Devices Year: 2016, Volume: 63, Issue: 9 pp. 3649 - 3656.

[13] M. Seif, F. Pascal, B. Sagnes, A.Hoffmann, S. Haendler, P. Chevalier, D. Gloria, "Study of low frequency noise in advanced SiGe: C heterojunction bipolar transistors", in Proc. ESSDERC, 2014, pp. 373-376

[14] J. Tang, G. Niu, J. D. Cressler, S. Zhang, D. L Harame, "Low-frequency noise figures-of-merit in RF SiGe HBT technology", IEEE MTT-S International Microwave Symposium Digest, vol. 1, pp. 179-182, 2002.

[15] Albert van der Ziel, Xiaonan Zhang, and Adam H Pawlikiewicz, 'Localization of 1/F Noise Sources in Bjt's and Hbjt's—I. Theory', IEEE Transactions on Electron Devices, 33 (1986), 1371-76.

[16] Jarrix, S., Delseny, C., Pascal, F., and Lecoy, G.: 'Noise correlation measurements in bipolar transistors. 1. Theoretical expressions and extracted current spectral densities', J. Appl. Phys., 1997, 81, (6), pp.2651–2657

[17] F. Pascal, J. Raoult, C. Delseny, P. Benoit, M. Marin, M. J. Deen, 19th International Conference on Noise in Physical Systems and 1/f Fluctuations, Tokyo, Japan, September 9-14, 2007,p 77-82.