Lorentzian Noise Approach for 1D Transport Studies

Mykhaylo Petrychuk
Bioelectronics (ICS-8)
Forschungszentrum Jülich
52425 Juelich,Germany
m.petrychuk@gmail.com

Ihor Zadorozhnyi
Bioelectronics (ICS-8)
Forschungszentrum Jülich
52425 Juelich,Germany
i.zadorozhnyi@fz-juelich.de

Yurii Kutovyi
Bioelectronics (ICS-8)
Forschungszentrum Jülich
52425 Juelich,Germany
y.kutovyi@fz-juelich.de

Siegfried Karg
IBM Research
Zurich, Säumerstrasse 4
8803 Rüschlikon, Switzerland
SFK@zurich.ibm.com

Heike Riel
IBM Research
Zurich, Säumerstrasse 4
8803 Rüschlikon, Switzerland
hei@zurich.ibm.com

Svetlana Vitusevich*
Bioelectronics (ICS-8)
Forschungszentrum Jülich
52425 Juelich,Germany
*s.vitusevich@fz-juelich.de

***Abstract*—Nanowire structures (NW) exhibiting one-dimensional (1D) transport properties are attracting increased interest within the scientific community due to their unique ability to improve carrier mobility and reveal new effects. This field of research provides an important guideline for the development of advanced devices. However, several issues related to exchange processes with traps have to be addressed before the full potential of 1D transport can be utilized at room temperature. We study the mechanisms of variability in InAs NW structures due to several traps with different characteristic time constants. We show that the Lorentzian noise component and the random telegraph signal noise can be effectively analyzed to confirm the formation of quantum transport in 20 nm diameter InAs NW structures.**

Keywords—1D transport, Lorentzian noise, nanowire

I. Introduction

InAs nanowires (NW) represent promising key materials for registering quantum transport properties [1, 2], which can be observed even at room temperature. At the same time, there are several related issues and one in particular needs to be resolved before the unique features of one-dimensional (1D) transport can be used for the development of information technologies. The main challenge is variability effects which deteriorate the stable quantum operation of such unique NW structures. As shown in [3], the traps in InAs NWs impact transport properties. Slow states with relaxation times in the order of minutes or even hours have a significant effect on the stability of the electrical characteristics of the samples. Detailed studies of slow states in a dielectric layer [3] involve measuring the magnitude of the hysteresis at room temperature. It is noted that relaxation of slow states occurs involving centers with different time constants. At the same time, the estimated density of slow centers substantially exceeds the density of fast centers by more than one order of magnitude. However, operation in that quantum regime close to room temperature has not yet been reported in the literature.

In this work, we demonstrate that the quantum operation regime can be achieved for InAs NW structures although there are a lot of traps influencing the behavior of I-V characteristics. In this respect, a powerful method of noise spectroscopy was used. We show that the analysis of random telegraph signal (RTS) noise and Lorentzian noise components can be used to study quantum conductivity in InAs NW structures with a diameter of 20 nm.

II. Experimental Details

The InAs nanowires under study were grown using metal organic chemical vapor deposition (MOCVD) technology. Nanowire structures with a diameter of 20 nm were coated with a 5 nm Al_2O_3 layer and transferred to a Si substrate covered with HfO_2 dielectric layer. Metallic contacts made of Ni were patterned in such a way as to obtain transmission line model structures (TLM). Such TLM structures allow us to study transport properties in nanowires of different lengths (Fig. 1). The silicon substrate was used as the back gate.

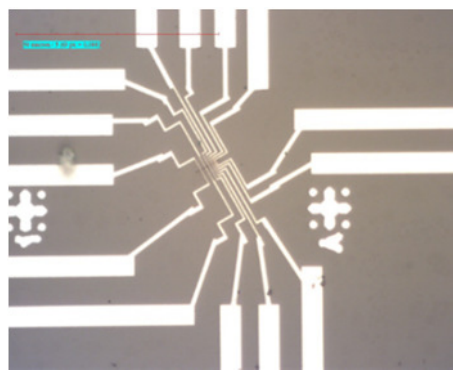

Fig. 1. An optical image of an InAs nanowire chip.

III. Results and Discussion

We investigated variability effects and current fluctuations in I-V characteristics of the fabricated InAs NW structures of different lengths: 3.0 µm, 1.2 µm, and 0.6 µm. Typical output characteristics $I_D(V_{DS})$ of the 3 µm long NW sample measured at different drain source voltages in the range $V_{DS} = 0 - 50$ mV and at different temperatures are shown in Fig. 2a. Each $I_D(V_{DS})$ dependence was recorded for 6 s.

Both sets of characteristics, measured in the absence of a gate bias (Fig. 2a) and when a voltage $V_G = 2$ V is applied (Fig. 2b), demonstrate the deviation from linearity of the dependences $I_D(V_{DS})$ when $V_{DS} > 10$ mV, i.e. an increase in the drain potential with respect to the source leads to a change in the charge state of the centers in the dielectric, which in turn leads to a decrease in the channel conductivity. Thus, not only the potential of the gate, but also the voltage across the channel of the InAs NW field structure increases the probability of free carrier trapping at the centers in the dielectric.

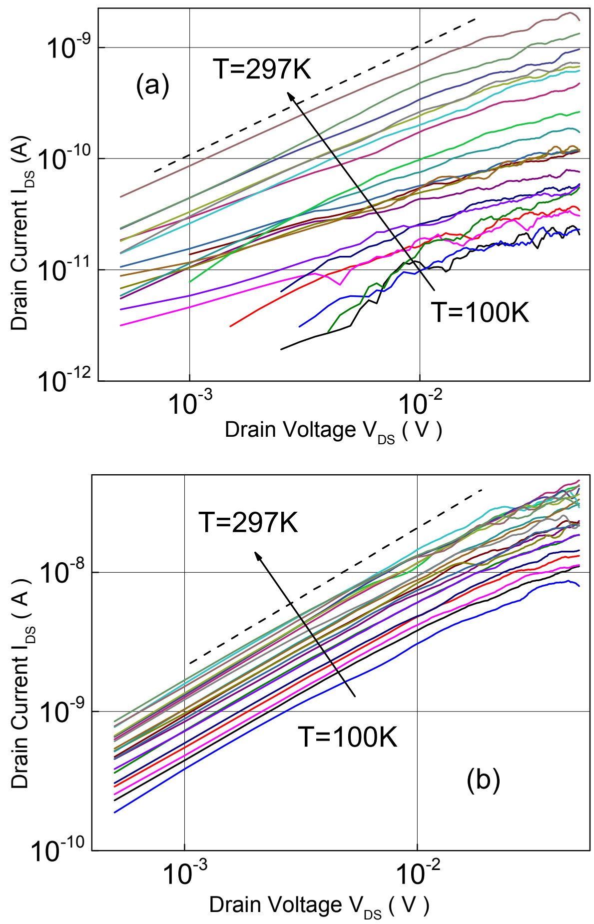

Fig. 2. $I_D(V_{DS})$ dependences of the sample with L = 3 μm at two gate voltages (a) $V_G = 0$ and (b) $V_G = 2$ V as well as at different temperatures in the range from T = 100 K to T = 297 K. The change step is $\Delta V_{DS} = 0.5$ mV. The curves are smoothed by the Savizky-Golay method, a second-order polynomial, and the window length is 15 points. The dashed line indicates a linear relationship.

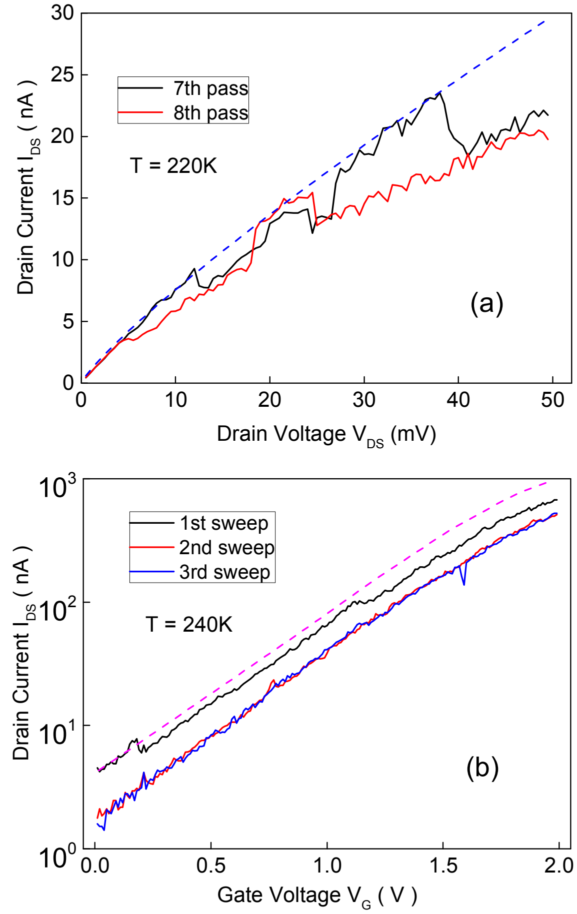

Fig. 3. Typical current-voltage (a) (V_G = 1.75 V) and drain-gate (b) (V_{DS} = 25 mV) characteristics of an InAs NW sample with length L = 3 μm, measured successively with a period of (a) 6 s and (b) 12 s. The dashed lines show the estimated curves in the absence of a current change. The measurement temperature is shown in the figure.

The nature of such captures can be traced by registering two typical dependences of the channel current on the V_{DS} channel voltage (Fig. 3a) and on the gate bias (Fig.3 b). As can be seen in Fig. 3b, the periodic application of voltage to the gate led to a gradual decrease in the channel current, first due to faster traps, and then due to slower ones. In this case, the step of decreasing the current, apparently caused by the capture of one electron, became an essential part of the total current. Changes in the current upon the application of V_{DS} are mainly due to thermal fluctuations and are smaller than the current changes upon the application of the voltage V_G. In the first case, the main role is played by faster transitions with characteristic times in the order of seconds.

Remarkably, random telegraph signal (RTS) behavior was registered in time traces of the NW structure. It should be noted that, in contrast to previously considered disadvantages of RTS its characteristic time constant can be used to obtain enhanced sensitivity biosensors [4, 5]. Thus, RTS component studies represent a powerful method for the stochastic and dynamic characterization of single traps.

Fig. 4 demonstrates typical time traces obtained for InAs NW FETs. Based on the results obtained with increasing gate voltage (Fig. 3b), it can be argued that the physical cause of the current change is the lowering of the potential barrier due to the trapping of electrons to centers in the surface dielectric when a voltage is applied both to the gate V_G and to the channel, i.e. drain-source voltage V_{DS} . This result is in agreement with observations reported in [3].

In addition, we performed measurements of conductivity as a function of temperature at different V_G and V_{DS} voltages. Fig. 5a shows the results obtained for V_{DS} ranging from 5 mV to 50 mV at gate voltage $V_G = 0$. Two sections of curves with different logarithmic slopes can be distinguished, which corresponds to two activation energies $\Delta E_1 = 0.20$ eV and $\Delta E_2 = 0.05$ eV. With an increase in the voltage V_G, the first section expands practically over the entire range of measurement temperatures, whereas the second section almost completely disappears.

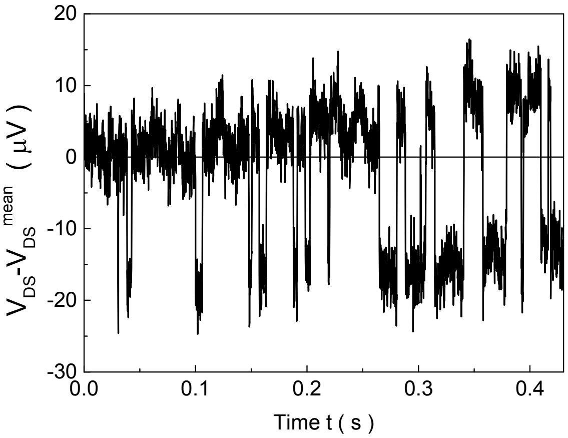

Fig. 4. Time trace demonstrating RTS behavior in the drain current of an NW sample (L = 3 μm), V_{DS} = 20 mV, V_G = 0, T = 220 K.

It could be assumed that at low temperatures shallow, and therefore faster, traps play a significant role in current changes and that with increasing temperature deeper (slower) traps prevail. For this reason, at low temperatures, the channel conduction time drift is insignificant and increases with increasing temperature. This is also due to the very "slow" centers, with time constants measured in hours, involved in the processes of changing the conductivity. The probability of capture/emission of electrons at slow centers increases with increasing V_{DS} and V_G . Thus, the mechanism of activation of the centers appears to be rather complicated as both thermal activation and electro-activation are present.

The dependences of activation energy ΔE_1 as a function of the gate bias V_G (Fig.5b) are plotted using the results of the temperature dependences of the conduction channel G (T) obtained for different gate voltages. The decrease of the energy ΔE_1 with increasing bias V_G supports the influence of the field effect on electron capture processes. Electron capture occurs with the participation of the field effect (Poole-Frenkel effect). The reduction in the height of the potential barrier ΔE_1 occurs according to the law:

$$\Delta E_1(E) = \Delta E_1(0) - A \times \beta \times \sqrt{E} \qquad (1)$$

where E is the field at the InAs / HfO_2 interface, β is the Poole–Franke coefficient, A is the dimensionless coefficient considering the geometric and dielectric parameters of the gate stack. The dashed line in Fig. 5b is plotted in accordance with Eq. (1) considering the relation $E \sim V_G$. The good agreement between the experimental data and the theoretical dependence confirms the significant effect of the electric field at the interface on changes in the conductivity of InAs NW.

The noise spectra measured at different temperatures allowed us to obtain an Arrhenius plot and therefore to calculate the activation energies of the active traps (Fig. 6). As can be seen, similar traps (see Fig. 5a) with an energy of 50 meV can be found using Lorentzian noise components in the spectra of InAs NW samples.

We revealed an important effect by analyzing Lorentzian noise components (typical noise spectra are shown in Fig.7a) in the sample with a length of 600 nm.

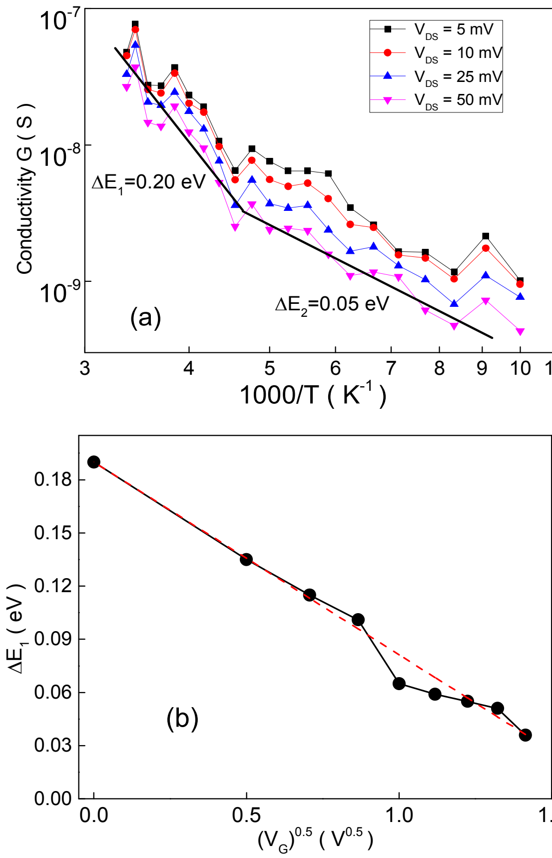

Fig. 5. (a) Temperature dependences of the conductivity of InAs NW with a length of L = 3 μm at V_G = 0 and several voltages of V_{DS} (indicated in the inset). (b) The dependence of the activation energy ΔE as a function of $\sqrt{V_G}$, obtained for $V_{DS} = 50$ mV . The dashed line indicates the calculated dependence obtained in accordance with Eq. (1).

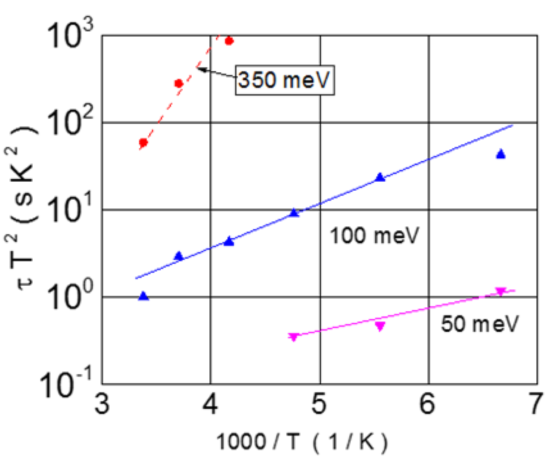

Fig. 6. Arrhenius plot obtained using noise spectra measured at differernt temperatures for the sample with L = 1200 nm.

The low-frequency Lorentzian noise plateau amplitudes, derived from the noise spectra, reflect the quantized behavior as a function of gate voltage (Fig. 7b). Moreover, similar behavior is also found in the time constant of capture–emission processes as a function of gate voltage thus confirming the characteristic synchronous patterns at room temperature.

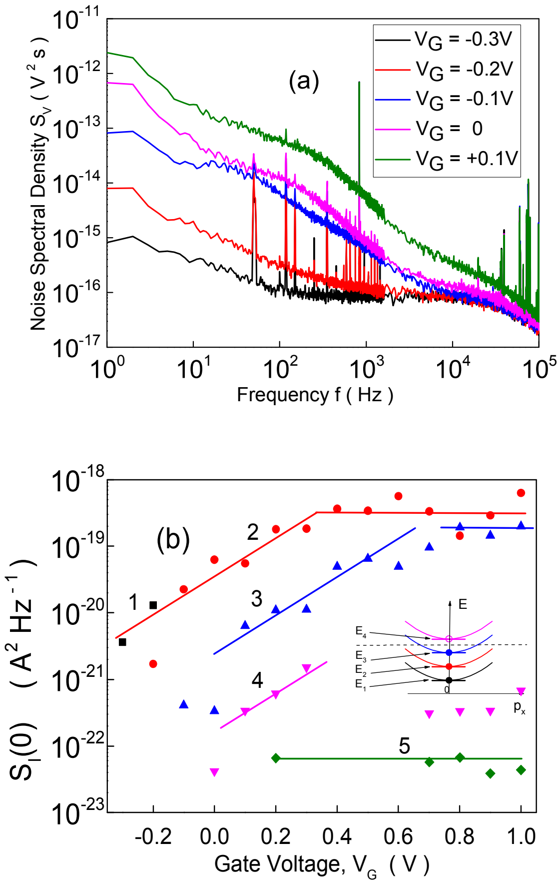

Fig. 7. (a) Noise spectrum of sample 5 (L = 600 nm), V_{DS} = 10 mV, V_G = -0.3 V to +0.1 V, T = 150 K; (b) the low-freqeuncy Lorentzian noise plateau values, S_I (0), extracted from measured noise spectra, as a function of gate voltage, T= 300K. The inset shows a schematic of the band structure with quantum levels of 1D conductivity in an NW structure.

The pattern revealed with respect to characteristic time behavior vs. gate voltage is explained in the framework of the model, taking into account the formation of band structure with several separate quantum levels. The inset in Fig. 7b shows a schematic of the band structure with quantum levels of 1D conductivity in an NW structure. Our estimations show that the Fermi wavelength is about 24 nm, which supports the quantization effect in the 20 nm diameter nanowire channels. The decrease in the threshold voltage with increasing temperature registered in the temperature range from 300 K down to 140 K additionally confirms the tendency for 1D conductivity to form on 20 nm diameter channels.

With increasing gate voltage, the number of conducting channels changes abruptly. The total conductivity is the sum of the quantum conductivities of the N channels and can be described by the following relation:

$$\sigma = \frac{e^2}{2p\hbar} \sum_N (1 - R_N) \quad (2)$$

where R_N is the reflection coefficient of the electron wave from the contacts.

Depending on the energy of the electrons, the specific quantum level and the degree of scattering, the coefficient R_N varies in the range of $0 < R_N \leqslant 1$.

This reflects the fact that electron exchange dynamics between the quantized levels can be analyzed even at room temperature using noise spectroscopy. The quantization effect becomes stronger with decreasing temperature, thus confirming that noise spectroscopy is a powerful advanced method for studying the formation of 1D quantum conductivity in nanowire structures.

IV. Conclusions

We investigated the transport and noise properties of InAs nanowire (NW) structures, currently recognized as a key material with potential for 1D transport at room temperature. The fine mechanisms for changing the conductivity of InAs NWs were investigated. It is shown that the application of a positive voltage to the drain-source contacts and to the substrate, which acts as a back gate, leads to a progressive capture of electrons to the centers in the gate dielectric at the InAs / HfO_2 interface. The time dependence of the degree of current change is non-exponential, which is determined by the participation in this process of centers with a wide distribution of time constants. Evidence is provided of conductivity jumps caused by the trapping of single electrons, which significantly changes the conductance of NWs. The physical mechanism that accelerates the capture of electrons at the centers by the application of an electric field is the Poole-Frenkel effect, which has been confirmed experimentally. Our results demonstrate that the Lorentzian noise component in noise spectra and random telegraph signal noise represents a powerful method for 1D transport studies in nanowire structures.

Acknowledgments

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