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Guest Editorial

Widespread media and communication applications are among the most demanding applications on current general-purpose processors and will continue to drive processor and system architectures in the next decade. In recent years, DSPs and general-purpose processors characteristics have got closer. General-purpose processors have been continuously integrating additional signal processing features and many of their new features have been defined to address media centric applications. In parallel, due to constantly evolving application requirements, many DSPs have become more flexible and are now able to execute a wide range of algorithms. Following this trend, the design of future processors and computing systems is tightly coupled with the design and development of emerging applications. On one side, processors and computing systems are designed to address the requirements of future applications. On the other side, applications very often have to be adapted to efficiently take advantage of processor and systems features.

This special issue proposes to address some of the principal technical challenges in the deployment of media and communication applications on general-purpose processors, by presenting research and development in both the hardware and software design issues. Most of the papers in this special issue are continuation of research topics presented in a special session of the IEEE International Conference on Multimedia and Expo 2002 in Lausanne, Switzerland.

The first set of papers of the special issue presents novel modeling and performance estimation methods for multimedia applications. The first paper, "A Platform Independent Methodology for Performance Estimation of Multimedia Signal Processing Applications", by Hans-Joachim Stolberg, Mladen Berekovic and Peter Pirsch, presents a methodological framework for performance estimation in multimedia signal processing applications, on different implementation platforms. It derives a complexity profile, that is specific to a particular application, but completely independent of its optimization degree and the implementation platform. The combination of this complexity profile with platform-specific data then allows to estimate application performance on different platforms. The evaluation of the methodology for an MPEG-4 ASP video decoder, on a specialized VLIW media processor and an embedded general purpose RISC processor, shows a high degree of accuracy in the performance estimation. The second paper, "A Simulation and Exploration Technology for Multimedia-Application-Driven Architectures", by Ivano Barbieri, Massimo Bariani, Alberto Cabitto and Marco Raggio, proposes an application-driven architecture design approach based on Instruction Set simulation. It focuses on interpretative reconfigurable Instruction Set Simulator, in order to support both multimedia application design, and architecture exploration. Together, the novel VLIW-SIM system presents very interesting features such as efficient host resource allocation, Instruction Set and architecture description flexibility, high simulation speed and good accuracy, that is evaluated with tests in three case studies. "MPARM: Exploring the Multi-Processor SoC Design Space with SystemC", by Luca Benini, Davide Bertozzi, Alessandro Bogliolo, Francesco Menichelli and Mauro Olivieri, develops a complete simulation platform for Multi-Processor Systems-on-Chip called MP-ARM, that is based on SystemC as modelling and simulation environment. MP systems-on-chip generally provide a high degree of flexibility, and efficient architectural solutions for supporting multimedia applications, and the proposed simulation environment turns out to be a powerful tool for the MP-SOC design stage. An example in the evaluation of architectural parameters and bus arbitration policies shows that the effectiveness of a particular system configuration strongly depends on both the multimedia application itself, and the generated traffic profile.

The second set of papers describes application-specific optimization methods, which allows to increase the multimedia application performance, while maintaining a quality-of-service level. In "An efficient Embedded Bitstream Parsing Processor for MPEG-4 Video Decoding System", Yung-Chi Chang, Chao-Chih Huang, Wei-Min Chao and

Liang-Gee Chen, present an efficient and flexible bitstream parsing processor, along with novel approaches to parse data partitioned bitstreams. An efficient instruction set, optimized for bitstream processing, is designed and integrated into an MPEG-4 video decoding system. The new system is shown to achieve real time decoding of MPEG-4 Advanced Simple Profile Level 5 sequences (i.e., 4CIF images at 30 fps and 8 Mbps). The following paper, "Memory Performance Optimizations for Real-Time Software HDTV Decoding", by Han Chen, Kai Li and Bin Wei, shows that the main bottlenecks in software HDTV MPEG-2 decoding are due to memory operations. They propose to exploit concurrency at MB level to alleviate these bottlenecks, and introduce an interleaved block-order data layout to improve CPU cache performance. Along with an algorithm that explicitely prefetches macroblocks for motion compensation, and interleaves decoding and output at the macroblock level, the optimization framework allows to decode and display HDTV resolution video at 62 fps on a 933 MHz Pentium III processor. "Reducing 3D Fast WT Execution Time Using Blocking and SSE", by Gregorio Bernabe, Jose Garcia and Jose Gonzalez, then presents an optimization of recently developed 3-dimensional video compression schemes. The authors describe the hardware and software interactions for this application on a general purpose processor. They propose to exploit the memory hierarchy of the processor and to reuse the computation results to limit the number of memory accesses, and floating point operations. Along with algorithm-specific optimization techniques, using both Streaming SIMD Extensions, and algorithm vectorization, they demonstrate a speed-up of 5 compared to fully optimized version issued from the Intel C/C++ compiler. Finally, the paper "Processor Enhancements for Media Streaming Applications", by Sébastien Bilavarn, Eric Debes, Pierre Vandergheynst and Jean-Philippe Diguet, addresses the problem of scalable multimedia data delivery to handled clients. It presents an impact study of scalable data representations optimized for Quality of Service, on processor architectures, to achieve the best performance and power efficiency. In the particular case of Matching Pursuit 3-dimensional video compression, it studies the first design steps of an efficient reconfigurable coprocessor, in order to cope with future video delivery and multimedia processing requirements. Architectures perspectives are proposed, with respect to low development cost constraints, and easy coprocessor usage with an original strategy based on hardware/software codesign.

The selection of papers in this special issue is addressing the wide range of challenges to design future generations of media and communication processor and system-on-chip architectures, from system design aspects to dedicated hardware and software implementation issues. We hope the reader will enjoy the wide spectrum of topics covered by the selected papers as well as the in depth research presented in each of the seven papers in this special issue.

Finally, the guest editors would like to thank all the authors, for submitting their great work to this special issue. Thanks also to the expert reviewers who greatly helped to yet improve the quality of this exciting special issue. We would like to thank Prof. Sun-Yuan Kung, the Editor-in-Chief, for approving this special issue, and the Editorial staff, Mrs Michelle Misner and Anne Murray, for taking care of all the details along the process of the special issue.

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he has been a Researcher in the Architecture Research Lab of the System Technology Labs, Intel Corporation, Santa Clara, California. Erics research interests include image and video coding and processing algorithms as well as computer architecture and parallelism. At Intel he has been working together with different processor teams and microarchitecture research groups on the definition of new media and communication features (including new SIMD and streaming instructions, multicore processors and low-power architectures) in the CPU and the chipset to provide better media application performance and end user quality of service with a given system and processor power envelope and/or energy budget. More recently Eric has been working on system-on-chip modelling, processor and system power estimation and architecture design space exploration for consumer electronics applications. He is a member of the IEEE, of the ACM and of the SPIE.
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In 2002, he was the general chairman of the IEEE International Conference on Multimedia and Expo (ICME 2002). He has been serving as Technical Program Area Chair of IEEE ICME 2004 and IEEE ICME 2005, and in the technical committee of several international conferences. He is an Associate Editor of the IEEE Transactions on Multimedia, and a member of the Editorial Board of the EURASIP Journal of Signal Processing. He serves as vice-chair of the IEEE Comsoc Multimedia Communications Technical Committee, and is a member of the IEEE Multimedia Signal Processing Technical Committee.
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