Contact effects, Stability and Noise Investigation in Organic Thin-Film Transistors

G. Giusi[1] (ggiusi@unime.it), G. Scandurra[1], S. Calvi[2], G. Fortunato[2], M. Rapisarda[2], L. Mariucci[2] and C. Ciofi[1]

1. Department of Engineering, University of Messina, Messina I-98166, Italy
2. Institute for Microelectronics and Microsystems, National Research Council, Rome 00133, Italy

***Abstract*—In this work we report on the results of Direct-Current (DC) and Low-Frequency Noise (LFN) measurements in p-type staggered top-gate Organic Thin-Film-Transistors (OTFTs). The analysis involves the effects of Source/Drain contacts and the stability characteristics of OTFTs induced by Gate and Drain bias stress. Noise data are interpreted in the context of a multi-trap correlated-mobility-fluctuations (CMFs) model, showing that noise is dominated by acceptor-like traps. The influence of noise sources at contacts is found to be negligible. However contacts affect the measured noise by a non negligible differential resistance. The product between the scattering parameter and the effective mobility $\alpha\mu_{eff}\approx 2\cdot 10^7$ cm^2/C, which measures the strength of CMFs, is similar to what reported for a-Si:H and much higher with respect to c-Si MOSFETs revealing a strong correlation between CMFs and the state of disorder of the active layer. Instability is observed in presence of Drain bias stress and for sufficient short channel length (<10μm). The measured shift in LFNMs appears correlated with the shift of the measured channel current. In the context of the CMF model the noise shift can be interpreted as due to the increase of $\alpha\mu_{eff}$ caused by the increased scattering between the charged channel carriers and the charged traps at the interface.**

Keywords— organic, OTFTs, low frequency noise, LFNMs, stability, contacts, LFN measurements, bias stress.

I. INTRODUCTION

As for c-Si MOSFETs, Low Frequency Noise (LFN) measurements have been largely used as characterization tool in order to investigate the material properties and conduction mechanisms in Organic Thin-Film-Transistors (OTFTs). However, noise modeling in OTFTs suffers for the fact that conduction mechanisms are still not collected in a general accepted framework. For this reason, OTFT noise models are borrowed from the c-Si MOSFET models. In particular, it has been found a higher level of 1/f noise in OTFTs with respect to c-Si MOSFETs [1-8]. This result has been interpreted as a higher defect density in OTFTs with respect to c-Si MOSFETs, due to the disordered structure of OTFTs. In most cases the measured data fits within the Hooge mobility-fluctuation (MF) model [1-3] while, in other cases, the number-fluctuation (NF) [4-6] has been used to interpret the measured noise. It should be pointed out that, in OTFTs, the LFN analysis is complicated by the non negligible influence of the contacts. It has been reported, in fact, that contacts are responsible for additional fluctuations which, in some cases and particularly for short channel devices, completely dominate the overall LFN at strong current intensity [1, 2, 9, 11]. In this work we report on the results of DC and LFN measurements in p-type staggered top-gate OTFTs. Measurements are performed by the integrated system reported in [11]. The investigated OTFTs are based on a small molecule organic semiconductor (SmartKem p-FLEX, 20nm thick) and the amorphous fluoropolymer gate dielectric Cytop™ (550nm thick, relative dielectric constant ~ 2.1). More processing details can be found in [7]. Basic LFN measurements are reported in Section II while the influence of the contacts is discussed in Section III. In Section IV the "contact-free" LFN measurements are interpreted in the context of a multi-trap correlated-mobility-fluctuations model. Another important electrical property of OTFTs is the stability of the electrical characteristics which has been investigated typically under constant Gate bias stress [12, 18]. However few works have been devoted to the effect of Drain bias stress. In Section V we study the Gate and Drain bias stability by means of conventional DC and LFN measurements. To our knowledge, this is the first report where noise measurements are used as tool to monitor the bias stress instability in OTFTs.

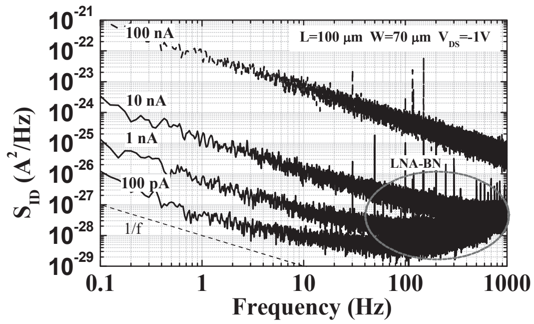

Fig. 1. Typical drain current PSD as function of the frequency f and of the drain current in linear regime. A clear $1/f^{\gamma}$, $\gamma\approx 1$, is observed from subthreshold to the strong accumulation region.

II. BASIC NOISE MEASUREMENTS

Fig. 1 shows the power spectral density (PSD) of current fluctuations S_{ID} as function of the frequency f in the linear regime for different values of the drain current, from the subthreshold to the strong accumulation region in a device with L=100μm. Noise measurements show a clear $1/f^{\gamma}$, $\gamma\approx 1$, behavior observed in all the investigated measurement bias ranges. Since we obtain purely flicker noise, we can conclude that noise is generated by a continuous distribution of defects. This is different from what is sometimes reported in the literature. Other works have in fact reported deviations from the pure 1/f spectrum that have been attributed to generation-recombination noise caused by traps at the grain boundaries of the active layer [6, 13]. The increase of S_{ID} at higher frequencies is due to the LNA background noise (LNA-BN).

III. INFLUENCE OF CONTACS ON LFNMS

In the linear region the PSD of the measured current fluctuations S_{ID} can be considered as due to the sum of a contribution coming from the intrinsic device, and a contribution coming from the contacts

$$S_{ID} = S_{I,CH}\left(R_{CH}/R_T\right)^2 + S_{I,C}\left(R_C/R_T\right)^2 \qquad (1)$$

where $S_{I,CH}$ and $S_{I,C}$ are the current PSDs associated to the intrinsic channel and to the contacts respectively, R_{CH} and R_C are the differential resistances of the channel and contacts respectively, and R_T=R_{CH}+R_C is the total differential device resistance. Since we are interested in the intrinsic noise component $S_{I,CH}$, we have to evaluate the impact of the differential contact resistance (R_C) and of the contact noise ($S_{I,C}$). Since $R_{CH} \propto 1/I_D \propto L$ while R_C is expected to be independent on L, the contact resistance can be extracted by linear extrapolation of R_T measured in devices with different L at the same Gate voltage overdrive [14]. Fig. 2(top) shows the total resistance and the extrapolated contact resistance as function of the Gate overdrive (V_{GS}-V_0). The contact resistance reduces with the Gate overdrive from ~$10^7\Omega$ in the subthreshold region to ~$10^5\Omega$ in accumulation. A similar behavior and order of magnitude for R_C have been already reported in [14]. As evident from Fig. 2, the total resistance in the shorter channel devices is significantly affected by R_C, especially in the strong accumulation region, while R_C is almost negligible in the subthreshold region. However, in longer channel devices, for instance L=100 μm, the contribution coming from R_C can be, to a first approximation, neglected since R_T>>R_C. In order to estimate the impact of the contact noise $S_{I,C}$, Eq. (1) can be written as

$$\begin{aligned} &S_{RT} = S_{RCH} + S_{RC} \\ &S_{RT} = \frac{S_{ID}}{I_D^2}R_T^2 \quad S_{RCH} = \frac{S_{I,CH}}{I_D^2}R_{CH}^2 \quad S_{RC} = \frac{S_{I,C}}{I_D^2}R_C^2 \end{aligned} \qquad (2)$$

where S_{RT}, S_{RCH} and S_{RC} are the PSDs (Ω^2/Hz) related to R_T, R_{CH} and R_C fluctuations respectively. As in the case of c-Si MOSFETs, it is reasonable to assume that $S_{R,CH} \propto L$. The physical origin of the contact noise (S_{RC}) is an argument still not clear. However, it is expected that, as in the case of c-Si MOSFETs, S_{RC} is almost independent on L. Based on these assumptions, S_{RC} can be extrapolated by the linear fit of the curve S_{RT} vs. L [9]. Fig. 2 (bottom) shows S_{RT}/L in all investigated devices as function of the Gate overdrive. The noise S_{RT} scales well with L, meaning that S_{RC} is negligible (<<S_{RCH}) in the whole bias range. In other works significant effects of S_{RC} have been reported in both staggered [10] and coplanar [9] OTFTs, possibly resulting in a not-negligible defect density in the contact region due to different materials and/or process. From the previous analysis it is apparent that, in all the explored bias range from the subthreshold to the strong accumulation regime, the contact noise S_{RC} can be neglected while it is necessary to take into account the differential contact resistance R_C, especially in the shorter channel devices.

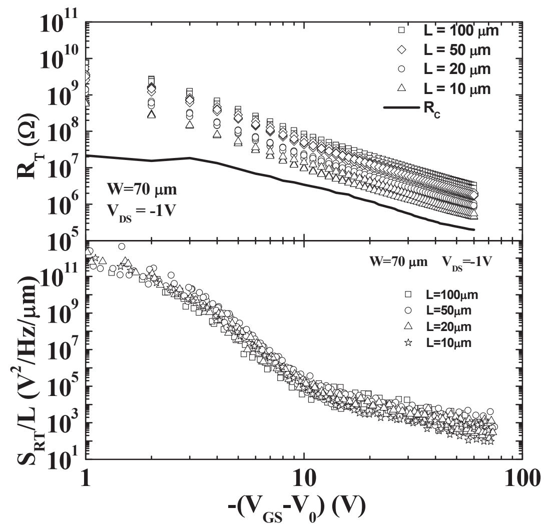

Fig. 2 (top). symbols: total resistance as function of Gate voltage overdrive for different samples with same nominal channel length (L); solid line: the contact resistance (R_C) calculated by linear extrapolation [14]; (bottom) scaled total device resistance PSD as function of Gate voltage overdrive for different samples with different L.

IV. NOISE ANALYSIS

Besides classical MFs and NFs, noise in MOSFETs has been also interpreted in a larger context by means of a correlated number fluctuation-mobility fluctuation (CMF) theory [15]. CMFs are different from Hooge MFs as they are due to the statistical fluctuation of the scattering cross section induced by the fluctuation of oxide charge which, in turn, is due to trapping/detrapping of charged carriers. For this reason the MFs are correlated with NFs. In the case of a pMOSFETs the model is

$$\begin{aligned} &S_{VG,CH} = \frac{S_{I,CH}}{g_m^2} = S_{VFB}\left[1 \pm \alpha\mu_{eff}C_{ox}\left(-\frac{I_D}{g_m}\right)\right]^2 \\ &S_{VFB} = \frac{kTq^2}{8WLC_{ox}^2}\frac{N_T(E_F)/\lambda}{f} \qquad \alpha = \frac{1}{\mu_{eff}^2}\left|\frac{\partial\mu_{eff}}{\partial Q_{ox}}\right| \end{aligned} \qquad (3)$$

where $S_{VG,CH}$ is the PSD (V^2/Hz) related to the equivalent intrinsic Gate voltage fluctuations, S_{VFB} is the flat-band Gate voltage PSD, μ_{eff} is the effective mobility in the active layer, Q_{ox} is the oxide charge density, α is a scattering parameter, k is the Boltzamann constant, T is the absolute temperature, q is the elementary charge, C_{ox} is the oxide capacitance, $N_T(E_F)$ is the trap density corresponding to the oxide energy level aligned with the Fermi level (E_F) in the active layer and λ is the tunneling parameter. The scattering parameter α takes into account for oxide-induced mobility fluctuations. In the CMF model (Eq. 3) $S_{VG,CH}$ is a quadratic function of the ratio I_D/g_m. In the case of donor traps (sign + in Eq. 3) $S_{VG,CH}$ increases with $-I_D/g_m$ (>0 for pFETs), while in the case of acceptor traps (sign - in Eq. 3) $S_{VG,CH}$ has a minimum, which is also a zero, with respect to $-I_D/g_m$. However, a zero in the measured noise is not possible from a physical point of view and it is necessary to admit a distribution of more dominant trap species, each of which is characterized by a couple of parameters N_{Ti} and α_i. In fact, if more trap species contribute

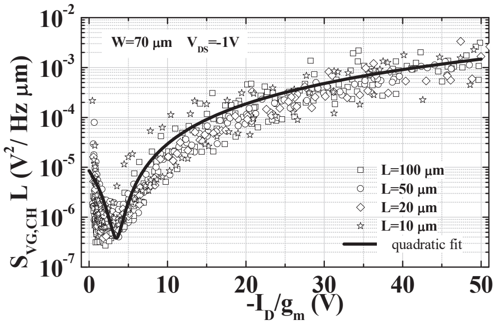

Fig. 3. symbols: $S_{VG,CH}L$ evaluated at f=1Hz as function of $-I_D/g_m$ in OTFTs with different L; line: quadratic fit according to the CMF model (Eq. 3).

to the Drain current fluctuations, the total $S_{VG,CH}$ can be calculated as the sum of the individual $S_{VG,CHi}$, because trapping/detrapping processes are uncorrelated. Since each $S_{VG,CHi}$ is a quadratic form, also the total $S_{VG,CH}$ is a quadratic form. Fig. 3 shows the "contact-free" geometry scaled $L{\cdot}S_{VG,CH}$ vs. I_D/g_m in devices with different L from 10µm to 100µm. The same figure shows a second order polynomial fit which is in good agreement with measured data. The measured data shows a minimum so that they can be interpreted in a multi-trap CMF context as discussed above. The presence of the minimum allows us to conclude that acceptor traps contribute to $S_{VG,CH}$ in the subthreshold region where $S_{VG,CH}$ decreases. However, we cannot exclude the presence of donor traps. In the strong accumulation region it is possible to make a linear fit of $S_{VG,CH}^{1/2}$ with respect to $-I_D/g_m$ meaning that, in this region, the noise is mostly due to a single dominant trap specie. Following this fitting procedure we obtained, from the statistical analysis of the different devices, the averages values of $N'_T=N_T/\lambda$= $3.2{\cdot}10^{12}$ cm^{-2}eV^{-1} and α=$1.6{\cdot}10^{7}$ Vs/C (with the sign – in Eq. 3). The extracted trap density is in line with other reports [6, 14] and it is much higher (assuming the same λ) with respect to conventional MOSFETs. The sign – in Eq. 3 means that, as in the subthreshold region, the noise in the strong accumulation region is dominated by acceptor traps. The scattering parameter value is much higher with respect to the case of (p and n type) MOSFETs (~10^7 Vs/C vs. 10^4 Vs/C). However the strength of CMFs is proportional to the value of the product $\alpha\mu_{eff}$. It can be noted that similar $\alpha\mu_{eff}$ –values found from the present analysis ($\alpha\mu_{eff}$~$3{\cdot}10^{7}$ cm^2/C) have been reported for a-Si:H TFTs [16] ($\alpha\mu_{eff}$=$2{\cdot}10^{7}$ cm^2/C) and are much higher with respect to the case of c-Si MOSFETs, although the mobility in c-Si MOSFETs is much higher than in OTFTs. These comparisons suggest a correlation between the state of order of the active layer and the relevance of CMFs.

V. Stability Analysis

The origin of instability in OTFTs, induced by bias stress, is not fully understood and it is generally attributed to trapping of channel charges into deep states in the semiconductor, at the interface with the dielectric or in the dielectric itself. For the stability analysis we have chosen a device with gate width W=200µm and a (relative) short gate length L=5µm. The measurement procedure consists in a sequence of 7 stress pulses (each 1000s in length) separated by DC and NOISE monitor operations (about 200s in length) so that Drain Current vs. Gate Voltage curves and NOISE measurements are recorded after each bias stress. In particular, the NOISE measurement is performed in a point in the strong accumulation region with a Gate voltage V_G = -15V and a Drain voltage V_D= -1V (the Source is always grounded). Different stress conditions are investigated varying $V_{G,stress}$ and $V_{D,stress}$. After the stress phase, the device is left to relax with V_G =V_D =0 for 7000s, while DC and NOISE are monitored as in the stress phase every 1000s. Fig. 4 shows the I_D-V_G curve of the fresh device along with the I_D-V_G after each stress pulse with $V_{G,stress}$=-30V, $V_{D,stress}$=-10V. It is clearly evident the instability of the investigated device due to the shift in the threshold voltage, as well as the degradation of the subthreshold slope and of the transconductance g_m (apparent increase). Since the (absolute) value of the Drain current reduces (increase of the threshold voltage), from a macroscopic point of view the instability could be attributed to positive charge trapping or positive charged defects creation at the interface between the semiconductor and the dielectric, or in the dielectric. The subthreshold slope degradation may suggest that traps/defetcts are located at the interface rather than in the dielectric bulk. Reverse I_D-V_G curves (not shown) have lower threshold shift, suggesting that traps/defects are preferably located close to the source region. Fig. 5 (top) shows the time evolution of the monitored current during stress ($V_{G,stress}$=-30V) for different $V_{D,stress}$, and during relax. It can be observed that i) the threshold voltage shift increases with $V_{D,stress}$, ii) the stress appears almost partially reversible since the monitored current comes back close to the fresh value. This last result may suggest that no (or few) new defects are created during the stress phase, and that the observed instability is caused by trapping (during stress) and release (during relax) of mobile carriers into trap sites located at the interface (source side). The instability increases with $V_{D,stress}$ for large $V_{G,stress}$ (as reported in Fig. 5) and also with $V_{G,stress}$ for large $V_{D,stress}$ (not shown). In particular no instability has been observed for large $V_{G,stress}$ and $V_{D,stress}$=0. This last result is in agreement with other reports where no Gate bias instability is observed for Cytop based OTFTs [17, 18]. Device simulations [19] show that the observed instability phenomena can be explained in terms of injection of high energetic carriers at the source side into the dielectric. In fact, carriers can gain enough energy due to the large depletion and consequent high longitudinal field at the Schottky contact between the source and the semiconductor. Fig. 5 (bottom) shows the normalized noise $S_{I,CH}/I_D^2$ monitored during the stress and relax phases. It can be observed that the noise increases during stress, and recovers during the relax phase, according to the current in Fig. 5 (top). As discussed in Section IV, the noise in the investigated devices can be interpreted in the context of the correlated-mobility-fluctuation model. Since the monitor bias is in the strong accumulation region,

$$\frac{S_{I,CH}}{g_m^2} \approx S_{VFB}\left[\alpha\mu_{eff}C_{ox}\left(-\frac{I_D}{g_m}\right)\right]^2 \rightarrow \frac{S_{I,CH}}{I_D^2} \propto N_T\left(\alpha\mu_{eff}\right)^2 \qquad (4)$$

that is the normalized noise $S_{I,CH}/I_D^2$ is independent on the bias and is proportional to $N_T(\alpha\mu_{eff})^2$. Let us notice that the increase of $S_{I,CH}/I_D^2$ cannot be explained with the apparent increase of g_m since $S_{I,CH}/I_D^2/g_m^2$ is not independent on the stress but reduces with it (not shown). Indeed, the apparent increase of g_m has been explained as an electrostatic effect due the presence of defected regions close to the contacts [20].

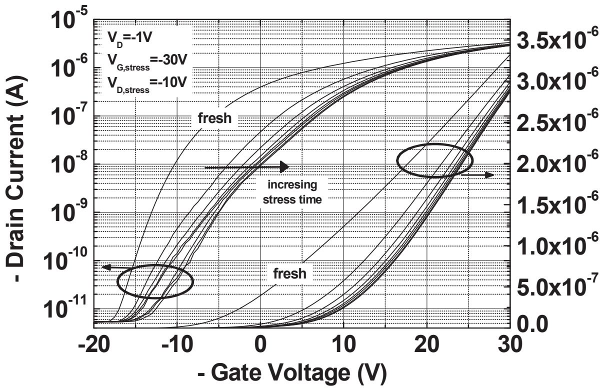

Fig 4. Drain current vs. Gate voltage (V_D = -1V) monitored during stress ($V_{G,stress}$ = -30V, $V_{D,stress}$ = -10V) every 1000s.

The effective mobility μ_{eff} can only reduce with stress, due to the increased electrostatic scattering between charged carriers and the traps/defects at the interface. The almost complete relax of $S_{I,CH}/I_D^2$ is not even consistent with a significant creation of new defects (N_T). The variation of $S_{I,CH}/I_D^2$can therefore be interpreted as due to the variation of the scattering parameter α (or $\alpha\mu$). In fact, the trapped charge during stress increases the coulombic scattering with channel charges with a consequent increase of α; during relax the noise $S_{I,CH}/I_D^2$ comes back to the initial value due to trap discharging and to the reduction of α. DC and NOISE measurements have been performed also in devices with a longer channel length (>5μm). No significant instability have been observed in DC and NOISE measurements in devices with L≥10mm for the same range of $V_{G,stress}$ and $V_{D,stress}$. This result is consistent with the hypothesis of trapping of high energetic carriers as contact effects and longitudinal fields are reduced in longer channel lengths.

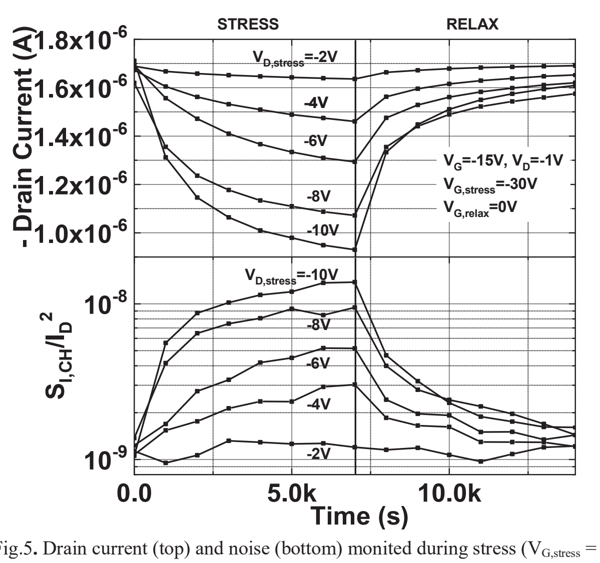

Fig.5. Drain current (top) and noise (bottom) monited during stress ($V_{G,stress}$ = -30V) and relax ($V_{G,relax}$=0) for different $V_{D,stress}$.

VI. CONCLUSIONS

LFN measurements show that the origin of current fluctuations in the investigated OTFTs can be interpreted in a context of a multi-trap correlated-mobility-fluctuations model, and that noise is dominated by acceptor-like traps. Contacts affect the measured noise only by a non negligible differential resistance. The higher scattering parameter found with respect to c-Si devices, can be used and interpreted as due to the higher state of disorder. Moreover, instability induced by Drain bias stress if found to be almost reversible and the related noise shift is found to be correlated with the shift of DC characteristics. This behavior can be interpreted as due to the higher scattering parameter caused by the increased scattering between the charged channel carriers and the charged traps at the interface.

REFERENCES

[1] P. V. Necliudov, S. L. Rumyantsev and M. S. Shur, “1/f noise in pentacene organic thin film transistors”, J. Appl. Phys, 2000, vol. 88, no. 9, pp. 5395-5399.

[2] L. K. J. Vandamme, R. Feyaerts and Gy. Trefàn, “1/f noise in pentacene and poly-thienylene vinylene thin film transistors”, J. Appl. Phys., 2002, vol. 91, no.2, pp. 719-723.

[3] O. Marinov et al., “Low-frequency noise in polymer thin-film transistors”, Circuits, Devices and Systems – IEE Proc., vol. 151, no. 5, pp. 466-472, Oct. 2004.

[4] S. Martin et al., “Flicker noise properties of organic thin-film transistors”,J. Appl. Phys., 2000, vol. 87, no. 7, pp. 3381-3385.

[5] Y. Xu et al., “Origin of low-frequency noise in pentacene field-effect transistors”, *Sol. State Elec.*, vol. 61, no.1, pp. 106-110, 2011.

[6] C. Y. Han, L. X. Qian, C. H. Leung, C. M. Che, and P. T. Lai, , “A low-frequency noise model with carrier generation-recombination process for pentacene organic thin-film transistor”, Jour. of Applied Physics, vol. 114, no. 4, pp. 044503, 2013.

[7] G. Giusi et al., “Evidence of Correlated Mobility Fluctuations in p-Type Organic Thin-Film Transistors”, IEEE Electron Device Letters, vol. 36, no.4, pp. 390-392 (2015).

[8] G. Giusi et al.,“Correlated Mobility Fluctuations and Contact Effects in p-Type Organic Thin-Film Transistors”, IEEE Trans. on Electron Devices, vol. 63, no. 3, pp. 1239-1245 , March 2016.

[9] Y. Xu et al., “Extraction of low-frequency noise in contact resistance of organic field-effect transistors”, Applied Physics Letters, vol. 97, no. 3, pp. 033503, 2010.

[10] Y. Xu et al., “Diagnosis of low-frequency noise sources in contact resistance of staggered organic transistors”, Appl. Phys. Lett., 98, 033505 (2011).

[11] G. Giusi et al., “Automatic measurement system for the DC and low-*f* noise characterization of FETs at wafer level”, IEEE I2MTC 2015, 11-14 May 2015, pp. 2095 – 2100.

[12] H. Sirringhaus, “Reliability of Organic Field-Effect Transistors”, Advanced Materials 2009, 21, 3859–3873.

[13] H. Kang, L. Jagannathan, V. Subramanian, “Measurement, analysis, and modeling of 1/f noise in pentacene thin film transistors”, Applied Physics Letters, vol. 99, no. 6, 062106, 2011.

[14] Y. Xu et al., “Modified transmission-line method for contact resistance extraction in organic field effect transistors”, *Applied Physics Letters*, vol. 97, pp. 063302, 2010.

[15] G. Ghibaudo, O. Roux, C. Nguyen-Duc, F. Balestra, J. Brini , “Improved analysis of low frequency noise in field-effect MOS transistors”, Phys. Stat. Sol. A, vol. 124, no. 2, pp. 571–581, 1991.

[16] E. G. Ioannidis et al., “Characterization of traps in the gate dielectric of amorphous and nanocrystalline silicon thin-film transistors by 1/f noise”, Journal of Appl. Phys, vol. 108, no. 10, pp. 106103, 2010.

[17] W. L. Kalb, T. Mathis, S. Haas, A. F. Stassen, and B. Batlogg, “Organic small molecule field-effect transistors with Cytop™ gate dielectric: Eliminating gate bias stress effect”, Appl. Phys. Lett. 90, 092104 (2007).

[18] M. Rapisarda et al., “Water stable Organic Thin Film Transistors (TFTs) made on flexible substrates”, Proc. Of the 15th IEEE Int. Conf. on Nanotechnology, Rome 2015, p. 1430.

[19] L. Mariucci et al., “High drain voltage induced instability in short channel staggered OTFT”, to be presented in International Tecnology Conference 2019.

[20] M. Rapisarda et al., “Electrical instability in self-aligned p-channel polysilicon TFTs related to damaged regions present at the gate edges”, Solid-State Electronics 52 (2008) 406–411.